Investigating the contribution of sealing chip application rates to the early failure of chipseals

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Abbreviations and acronyms

AADT	annual average daily traffic
AGD	average greatest dimension
ALD	average least dimension
BSM	*Bituminous sealing manual*
BWP	between the wheelpaths
CL	centreline
EL	edgeline
HCV	heavy commercial vehicles
IWP	inner wheelpath
NZTA	NZ Transport Agency
OWP	outer wheelpath

Contents

Executive summary

Amongst experienced practitioners, the general consensus on chip application is that a complete stone mosaic is the optimum, and it is better to apply extra chip than to leave gaps in the sealing chip mosaic. This has resulted in a general tendency for the industry to over-apply chip by an estimated 10%, to make sure there are no gaps in the stone mosaic. Experts in New Zealand and around the world cannot agree on chip application rates, how to measure them, and how to specify them.

The objective of this research, which was carried out between July 2006 and December 2009, was to investigate the effect that different application rates of sealing chip have on chipseal performance in New Zealand. Seven chipseals with varied chip application rates were constructed in various locations around the country, and the effect of the different chip application rates on the performance of the seals was monitored.

The seven chipseals (four single-coat seals, two drylock seals and one two-coat seal) were constructed on sites that had a range of traffic loadings but were generally straight and flat. The chip application rates constructed ranged from 'very very light' (VVL) to 'very heavy' (VH), and all were represented on most sites.

The different chip application scenarios (frames) monitored totalled 484 and provided a significant amount of data. The monitoring of these 484 frames showed that the chip application rate on the mostly low-stress chipseal sites did not directly affect chipseal performance in the first two years after construction (the monitoring period of this research).

Traffic volumes, traffic distribution and the existing surface condition had a significant effect on texture change, binder rise and chip breakdown within the monitoring frames.

The conclusions and recommendations of the research were as follows:

- Millions of dollars is wasted every year because excess chip is used during the construction of chipseals. Extra costs include the cost of the chip, transport costs, sweeping costs and windscreen repair costs.
- Chip application rates that are generally higher-than-required are targeted by both contractors and site engineers to ensure there are more than enough loose chips on the chipseal surface to complete the chip mosaic during trafficking. This has been identified as wasteful and adding cost, so the industry should agree to target lower chip application rates than the current practice.
- Incomplete chip coverage does not cause early chipseal failure in the low-stress environment.
- On low-stress sites, the target chip application rate should be reduced so that the aim is to apply the exact amount required, with no wastage of chip.
- The New Zealand chipsealing industry needs a specification that includes actual chip application rate targets in New Zealand, and an accepted method or tool to accurately measure the application rate.
- Further investigation should be carried out on chipseals undergoing higher traffic volumes and higher stress, to ascertain what effect the chip application rate has on their performance.

Abstract

Chipsealing is the predominant resurfacing used on the state highway network in New Zealand. An important component of chipseals is the sealing chip layer that is applied to protect the binder layer and provide surface texture and surface friction. There are a number of specifications written to ensure that the sealing chip used is the correct size and shape, and that it has the appropriate 'polished stone value' (PSV), but no specifications on chip application rates exist. Early-life failures of chipseals are generally attributed to the binder, the binder application rate, or the weather; however, the sealing chip application rate may also contribute significantly to these early failures.

The objectives of this research, which was carried out between July 2006 and December 2009, were to:

1 determine the effect of variations in chip application rate by constructing several seals with varied chip application rates, and monitoring the performance of the seals for two years

2 assess the effect of the time of sealing (in terms of season and weather) with chip application rates and the success rate of the chipseals

3 develop a pictorial and quantitative guideline for the correct application rate for sealing chip in New Zealand.

This report documents the performance, over the first two years after construction, of chipseals that were constructed using different chip application rates.

1 Introduction

With the vast majority (90%) of New Zealand roads surfaced with chipseal, it is very important that the application of sealing chip is optimised to ensure the best performance of the chipseals and minimise the waste of this non-renewable resource.

The purpose of this research project was to identify optimum sealing chip application rates and develop a guideline that will enable contractors to determine the appropriate sealing chip application rate.

Along with seal design and binder application, chip application is a critical part of chipseal construction; however, there is no simple method of accurately controlling chip application rates.

The problem is that the production of chip leads to variation in chip size and shape. These variations are caused by one or more factors, including:

- the quality and size of the feed rock
- feed rates into the crusher
- the cleanliness and degree of wear of the sizing screen
- wear of the crushing and shaping plant.

Normal practice to quantify coverage is to use an estimate of the area covered (in square metres) for the volume or mass of chip used (in cubic metres). An example is the New Zealand standard measure of m^2/m^3. However, variations in chip size and shape mean that application rates stating an 'area per square metre' are only applicable for each stockpile of each chip size. Using a weight or volumetric chip application rate target for chip that is of the same grade but has a different size or shape will result in over-or under-chipping.

In an effort to improve consistency in chip application from site to site and contractor to contractor, photographs were added to the New Zealand *Bituminous sealing manual* (BSM) (Transit NZ 1993), showing a range of chip application rates – those considered to be optimum; 10% and 20% below optimum; and 10% and 20% above optimum. These photographs were made available to sealing crew field staff, who tried to visually match what they achieved on site with what was on the provided photographs. It proved to be very difficult for them to consistently achieve a good match, partly because of the poor performance of most of the chip application devices used by contractors.

The practitioners involved in compiling information for the 2005 textbook *Chipsealing in New Zealand* (Transit NZ) decided that based on their recent experiences, the photographically depicted application rates in the BSM 1993 were 10% too heavy.

There is anecdotal evidence of significant disagreement between experts about the correct chip application rate during construction, the optimum rate of chip retained after 12 months of trafficking, and whether chip application rates are generally too high.

High chip application rates give rise to several extra costs – for removing the excess chip, of the wasted chip, and for disposing of the contaminated wasted chip material. This should provide an incentive for contractors to improve their chip application methodologies.

In addition, anecdotal evidence also suggests that the over-application of sealing chip during construction of the chipseal contributes to the early failure of chipseals.

The production and implementation of a sealing chip application guideline will reduce the cost of chipseal production by reducing sealing chip usage and wastage, and improving the success rate of chipseals.

2 Literature review

One of the aims of this research was to use past knowledge as the basis for the new guideline. However, there has been very little research carried out on the topic of optimum chip application rates. When designing chipseals for New Zealand, the industry has focused on the accuracy of the binder application rate, using only a simple calculation (based on generic chip application rates), to order chip quantities.

Most design methods for single-coat seals include the volumetrics of the chip layer, which is based on a single layer of chip lying with its shortest axis (the average least dimension, or ALD) vertical, with some spaces in between the chip.

However not all ALD measurements are the same. The ALD is measured by a calculation based on the particle size distribution, and is not an actual measurement.

Mackintosh (1961) concluded:

> *Surplus chips are not only whipped off by traffic, but actually cause the loosening of some chips already held by the binder …. Therefore, excess chips should **not** be applied as an allowance for whip-off. The aim should be such accurate rates of spread and spray that there is practically no whip-off. The only allowance to be made should be … for handling losses and imperfect workmanship.*

McLeod (1969) studied and compared seal design methods from around the world, and concluded:

> *... A careful investigation and comparison of several methods has shown that they do not agree among themselves, and that for some of them the amount of cover stone is too little, while the quantity of asphalt binder stipulated is excessive.*

In *TRL road note 39* (TRL 1972) the main paragraph in a section on chip application stated:

> *Rate of spread of chippings. The quantity of chippings must be sufficient to cover the entire surface of binder film after rolling. The most reliable way of ensuring a complete cover is to lay a slight excess of chippings.*

Major and Tuohey (1974) discussed optimum chip application rates as follows:

> *The chip spread rate is just sufficient to produce a uniform mat one stone deep in shoulder to shoulder contact after rolling. Such a spread rate usually appears insufficient until rolling operations have oriented the chips with least dimensions vertical.*

When discussing chip application rates, Potter and Church (1976) wrote:

> *Little mention … of aggregate application rates. This is for two reasons:*
>
> *(a) The application rate of aggregate is less critical than that of binder, and*
>
> *(b) There are only two criteria of real importance. One is the ALD and the other is the loose layer depth.*
>
> *Perhaps the most important fact about aggregate application rate is that an excess is merely wasteful, but insufficient can be disastrous. Provided any excess aggregate is carefully swept off …. If insufficient aggregate is used … the air voids will be large, the chippings not firmly held and stripping will occur.*

They also developed the following formula for calculating the appropriate chip application rate:

Aggregate application rate = $\frac{1000}{1.4 \times ALD}$ *add 3% for whip-off allowance*

To design both single and double seals, Semmelink (1987) used a rational approach based on the modified tray test. He used the data from the tray test to calculate the required aggregate application rate, but his work was focused on the design of the binder application rate. One comment of note was:

> *… there is a wide scatter in the case of the actual void content.*

Most design systems rely on a constant voids value for the target aggregate application.

Houghton (1987) analysed single-coat seal design and made the following comments in his paper about chip application:

> *More chip: more voids.*
>
> *Providing the shape of chips, whether small or large, and the chip application rate is constant, the volume of voids in a chip seal at any time will be dependent on the size of the chip and the amount of compaction the seal has had …*

He concluded that:

> *The volume of voids in a seal, and thus the binder application rate required to produce a successful seal, is not only related to the size of the chip (ALD) but is also related to the chip application rate.*

His recommendations included the following:

> *For any particular sealing chip it is recommended that an application rate be determined by observations and measurement and that the application rate be adhered to at all times.*

Sheppard (1989) recommended:

> *… when the real cost per m² is compared the costs are much closer. There are also other costs if extra chip is applied; the cost of extra sweeping, extra spreading costs, and extra disposal costs.*

Dickinson (1990) analysed close packing of particles and concluded that:

> *… For single seals laid on hard smooth surfaces the packing is orthogonal or more open than orthogonal and the particles are aligned with a flat side roughly parallel with the substrate surface. Layer thickness may not be significantly greater than the aggregate ALD.*

Petrie et al (1990) investigated chipseal compaction and noted:

> *It would appear that over chipping extends the time taken for redistribution of loose chip; i.e. the rate of change under compaction is slower than for optimum or underchipping ...*

and:

> *There will always be areas devoid of chip after the initial chip application, regardless of the application rate, using the best of conventional equipment – unless the application rate is grossly excessive. However, these voids are relatively quickly filled under moderate vehicle trafficking by redistribution of loose chip, not previously in contact with the binder, and to a relatively lesser extent by lateral displacement (i.e. squeezing sideways) of embedded chip.*

Conclusions from their research included:

(a) By far the most significant changes in chip embedment and displacement (to infill the "windows") occur under the first 2 hours of trafficking.

(b) … There is difficulty in maintaining a consistent chip spread rate, even by an experienced contractor under research conditions ...

Recommendations from their research included:

- *That trials be established to determine optimum chip spreading rates and construction practices.*
- *…That more effective means of redistributing loose chip be investigated ...*

Major (1993) carried out an investigation in New Zealand into a high incidence of chip loss from reseals carried out the previous season and concluded:

It is clear from the field observations that the volume of voids in a chip layer depends upon more than just the average least dimension (ALD) ...

and:

At most sites, the binder rise was less than expected. This appeared to be caused by excessive chip application rates that prevented the chips bedding down with their least dimensions vertical.

A number of influences are believed to have led to this situation, including:

(a) Acceptance and approval of a coarse texture without recognising that the coarse texture may be the result of limited embedment caused by overchipping.

(b) In many cases, a deliberate choice by consultant or client to have substantial chip present at the stage that rolling is completed and the contractor plant leaves the site.

(c) Absence from sealing specifications of quantitative measures that discourage overchipping.

(d) Limited responsibility/maintenance periods (seven days to three months) on many contracts so that overchipping is contractually acceptable.

(e) Reduction in specified rolling, so that initial uncontrolled speed trafficking takes place earlier. Overchipping seems more likely to survive than underchipping with limited rolling.

(f) When using chip spreaders which do not have a reliably uniform discharge, a tendency is to apply "enough so that we don't have any deficient areas".

(g) Near total absence of the use of "hand spotting" on areas that have been identified as having initial under application of chip.

The BSM's (Transit NZ 1993) discussion of chip application stated:

Research in New Zealand into the appropriate chip application rate has not been carried out to the same extent as has research into binder application rate ...

and:

A commonly used relationship … has been:

Chip application rate = 630/ALD.m^2/m^3

which was considered to result in an approximate 5% excess of chip.

Hand placing of chip and visual assessment on samples … suggest a theoretical optimum application rate relationship:

Theoretical application rate = 1000/ALD.m^2/m^3

Limited investigations have also shown that chip application rates in the field can be variable even when closely supervised. The extent of this variability is within the range of the above two relationships.

Gaughan and Jordan (1994) said:

… generally binder rates and aggregate spreading rates are not critical …

Rolling and traffic action does not greatly alter the voids in the aggregate mat unless the seal fails …

Holtrop and Loughran (1994) said:

… the rate of application did influence the seal coat mosaic … the lighter application resulted in a better mosaic and less breakdown … The trial sections spread at the lighter rate appear to be performing as well as the rest, and this tends to further confirm that the normal tendency is to overspread.

… At the accepted standard rates the aggregate particles do not orient themselves, as expected, with the least dimension vertical. At the lighter rates the particles do more closely conform as expected.

Gaughan et al (1996) said:

… Uniform spreading of the aggregate particles at the specified design rate is essential to obtain an interlocking aggregate mosaic, which is important for the long term service performance of a seal.

In a Victorian (Australia) sprayed-seal contract document (Vic Roads 1999), the contractor is penalised for being >5% below the design rates of application of aggregate, but there is no penalty for being higher than the design rate. This would obviously drive the contractor to err on the high side of aggregate application.

TRL road note 39 (TRL 2002) only provides guides for aggregate application rates – it does not provide a formula or specification. The guide does suggest over-applying the second coat of chip at intersections, in order to minimise traffic damage.

The Caltrans *Technical advisory guide* (2003) states:

Calculation of the design aggregate application rate is based on determining the amount of aggregate needed to create an even, single coat of chips on the pavement surface.

In 2005, Transit et al (2005) produced the *Chipsealing in New Zealand* textbook. The textbook provides a new calculation for chip application rates that reduces the target application rate, but is based on the ALD of the chip. The variation in the shape of the chip is not accounted for in the calculation. Also included in this discussion is the allowance for an extra 10% of chip that is 'whipped off' in the first 48 hours after construction. It is suggested that the rates should be decreased slowly, calculating the spread rate by area covered divided by the volume of chip used.

The textbook includes some updated photos of what the target application rate should look like. The photos used are the same photos used in the BSM 1993 edition, but they are re-labelled – the photo that was originally labelled as showing 10% too little chip is now classified as 'optimum chip application', and the photo that was originally labelled as optimum is now classified as having 10% too much chip applied.

In the 'Seal design' section, the textbook discusses previous research and manuals and provides this formula for calculating the chip rate:

$$Rate = \frac{750}{ALD}\ m^2/m^3.$$

> *This allows for approximately 10% for whip-off but assumes a good standard of uniformity of chip spread.*

The textbook also discusses different chip application rates for other seal types, such as 'racked-in seals', 'two-coat seals' and 'sandwich seals', as well as the importance of chip combinations.

2.1 New Zealand industry practice

After discussions with many of the experienced sealing practitioners from throughout the New Zealand chipsealing fraternity regarding chip application rates, it seems that the calculations in the review above are generally used to order the correct quantity of chip. However, the calculations do not take into account other variables such as chip shape, chip range, precoating, traffic, binder etc, so it they are only a starting point for calculating the optimum chip application rate for a site.

Current practice is that the target chip application rate is established and agreed with the supervisor by visual assessment on site. Once agreed, the plant operators and chip runners can establish the target speeds and settings that will produce the required chip application rate that they will adhere to until the target rate is changed.

2.2 Summary of literature review

In summary:

- There are many methods used to calculate the optimum chip application rate. Most are based on applying enough chips to cover the surface 100% with chips lying on their greatest dimension (ie their ALD is vertical) and shoulder-to-shoulder after compaction and trafficking.
- The over-application of chips may be detrimental to seal performance.
- Over-application of chips is wasteful and expensive.
- There is very little agreement amongst the experts on what the optimum chip application rate should be – what it should look like, how to specify it, how to measure and control the chip application rate during construction, and how much (if anything) to allow for 'whip-off'.

3 Methodology

3.1 Identify trial sites

A research steering group including representatives of the NZ Transport Agency (NZTA), Roading New Zealand and local authorities was set up to help identify several trial sites for the project.

The main requirements for the sites were that:

- the existing surface had a consistent texture that was suitable for resealing
- the site was straight and flat
- the appropriate reseal treatment was a single-coat grade 3 chipseal.

Although the number of sites available for selection was limited because of the above site requirements, six sites around the country were identified as suitable, and seals on these sites were constructed by various Fulton Hogan crews (apart from the Motukarara site, which was constructed by an Isaac Construction crew).

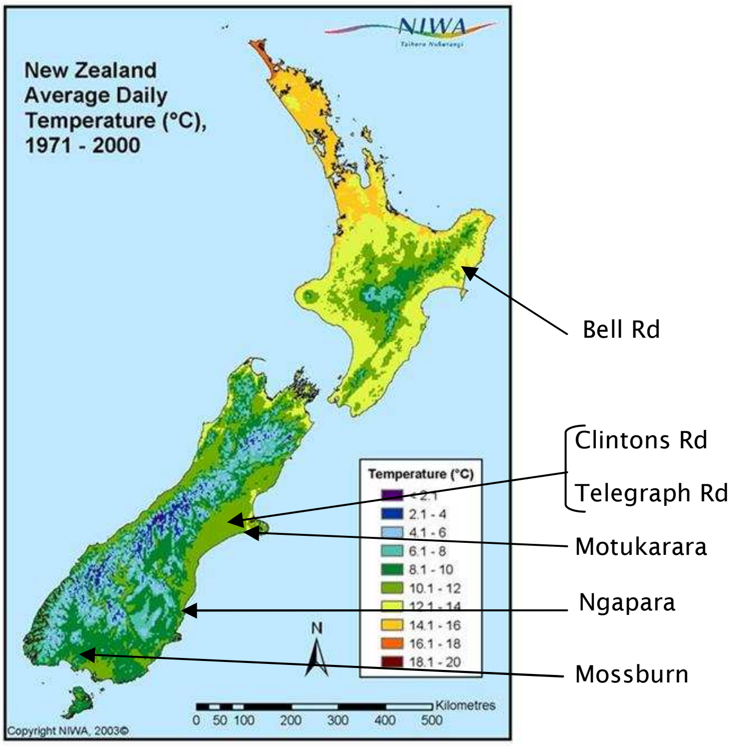
The sites were located in Gisborne (Bell Rd), Mossburn, Ngapara (Whitestone Rd), and Canterbury (Clintons Rd, Telegraph Rd and SH75 near Motukarara).

Most of the seals were single-coat grade 3 chipseals. However, both Bell Rd and Mossburn had a ‘drylock’ chip layer applied, and a second adjacent site at Mossburn was a two-coat seal.

The sites provided a good geographic spread and a range of climates (see figure 3.1).

The traffic levels varied from a high of 5471 annual average daily traffic (AADT) with 17.5% heavy commercial vehicles (HCV) on Bell Rd, to a low of 126AADT (0%HCV) on Clintons Rd.

Figure 3.1 Test site location map



3.2 Construction of trial sites

The sites were prepared for chipsealing as part of the various contractors' normal resealing methodologies. The seal designs for binder application rates were calculated by the contractors or the consultants as required under their contract conditions.

The contractors sprayed the binder as normal, using normal spray-run lengths. Samples of the binder and copies of the spray sheets were taken from the sprayers at the end of the spray run.

Samples of the sealing chip were taken from the chipspreaders/roller spreaders at the start of the runs. These were tested to measure the actual size, shape, and average weight (per chip), of the sealing chip used in the trials.

The only difference for the sealing crews was the paint marks indicating the target chip application rates for each section (see figure 3.2). The chip runners or operators were asked to spread the chip aiming for the range of chip application rates that they would normally use. The targets were 'very light' (VL), 'light' (L), 'normal' (N), 'heavy' (H) and 'very heavy' (VH). On some sites the application rates were on the light side, so those sites ended up with some areas with a 'very very light' (VVL) chip application rate; and some sites had no 'very heavy' areas because the chip was not applied heavily enough.

The trial layouts aimed to have the light application rates upstream to avoid chip being imported from the heavier sites onto the lighter sites. This was achieved on most sites and the frames were labelled as per the targets, regardless of the actual application rate. Some of the monitoring frames were chosen based on assumed wheelpath locations and visual assessment of the achieved chip application rates, to get a range of chip application rates.

A 'very very light' rate was added after it was found that some areas had a chip application rate that was as light as could be achieved without causing vehicle tyres to pick up binder from below. This happened on very small, isolated areas on some of the sites, such as at Clintons Rd (see the site layout in figure 3.3).

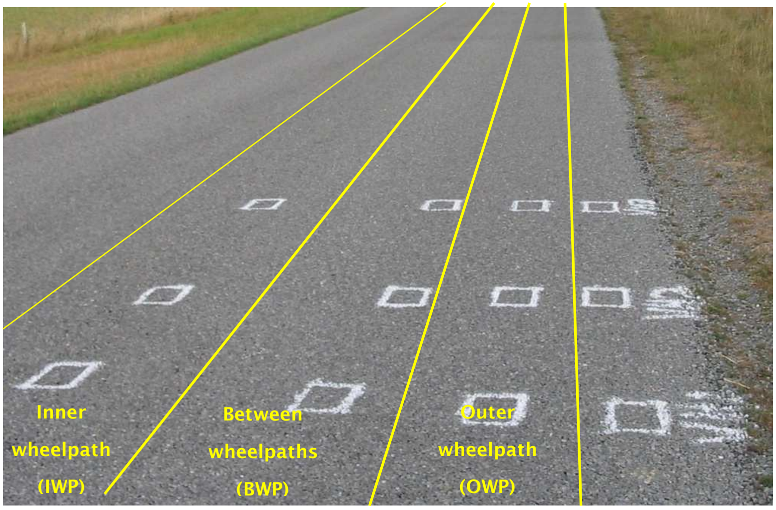
The 'normal' rate was the application rate that the chip runners would normally be spreading according to their agreement with the supervisors. The 'very heavy' rate was as heavy as could be achieved without a double layer of chip, in order to avoid the problem of chip crushing.

As the normal construction flow was disrupted by the construction of the trial sites, it was decided that a control section for each site should be located away from the main trial sites. This location was chosen after the seal construction was completed, and was assumed to be the application rate that the teams would have normally applied if they hadn't been disturbed by the research.

The monitoring areas were selected and the frames marked within each section – the frames were chosen to represent the target chip application rate for that section.

Figure 3.2 Target chip application rate marked for operator

Figure 3.3 Clintons Rd very heavy (VH) chip application site marked out



3.3 Trial sites

3.3.1 Clintons Rd

3.3.1.1 Test site layout

The Clintons Rd sealing chip was applied in one spread using an Etnyre Chipmaster chipspreader, which covered the entire lane width from seal edge to centreline (CL). However, issues with a sensor meant one half of the box was spreading more heavily than the other.

Marks were painted on the road so that the operator could change for the various target application rates on the run by winding the rate up or down on the control. There was a delay between changing the control and the rate actually changing, but it all worked well and the site ended up with a good range of chip application rates.

As with all sites, the crew endeavoured to have the lighter application rates at the start of the site, getting progressively heavier through the normal application setting until there was excess chip being applied. The chipspreader operator was then left to reset and carry on as normal, before choosing a small section away from the managed trial site to be the control section. The chip application rate for the control section was similar to the setting of the 'normal' section. This confirmed the consistency of the chipspreader settings. The chip application rate on the heaviest frame was more than 2.5 times that of the lightest.

Table 3.1 Clintons Rd site layout

Clintons Road site layout												
		Control (C)		Very heavy (VH)	Very light (VL)	Very very light (VVL)	Light (L)	Very very light (VVL)	Normal (N)	Very very light (VVL)	Heavy (H)	
Hororata	Left shoulder	☐		☐	☐		☐	☐	☐		☐	Burnham
	Left OWP	☐		☐	☐	☐	☐		☐		☐	
	Left BWP	☐		☐	☐	☐	☐		☐		☐	
	Left IWP	☐		☐	☐		☐		☐	☐	☐	
	Right IWP											
	Right BWP											
	Right OWP											
	Right shoulder											

3.3.1.2 Road layout and traffic

The Clintons Rd site was flat and straight, with a hedge on the north side of the road providing shade though most of the day during winter. The road was not roadmarked and had an average width of 6.82m from edge of seal to edge of seal.

The AADT was low (estimated at 126vpd with 0%HCV), so there was very little compaction by the traffic, and the binder application rate was set high at 2.8–3.0 l/m². Because the road had no centreline, the traffic tended to travel down the centre of the road, forming three reasonably defined wheelpaths, and the shoulders received very little traffic (see figure 3.4). The middle wheelpath was located close to the centreline of the seal.

Figure 3.4 Clintons Rd site looking east towards Burnham (16/12/08)

3.3.1.3 Construction

The seal was constructed in early February in fine, warm weather. The seal had plenty of time to settle down before the winter frosts arrived.

There was a lot of chip movement during the first week, which was probably related to the sweeping of the site moving chip around so that it fell into the gaps left during construction.

3.3.2 Motukarara

3.3.2.1 Chip application

The Motukarara sealing chip was applied by the Isaac Construction crew, using roller spreaders. The application rate on the inner wheelpath (IWP) was from a different run than the other three locations and in some areas was affected by overlap, which resulted in a heavier chip application rate than at the other locations.

There was some binder rise on the existing surface where the 'heavy' and 'very heavy' sections were constructed.

The initial locations chosen for the outer wheelpath (OWP) test frames in the 'normal', 'heavy' and 'very heavy' sections were too close to the edgeline and were covered with paint when the edgeline was roadmarked. The initial photos for the between the wheelpaths (BWP) locations were used, and new frames were marked for the IWP at these locations. The initial data for these frames was estimated from the next photo and frames with similar numbers of chip.

The chip application rate was varied well by the chip runner and he was able to construct the largest range of chip application rates of all of the trial sites. The lightest rates were at the start of the site, with increasing rates until the end.

The overlap of the two roller spreader runs provided some spare chip that was moved into the outside frames by sweeping and traffic movements.

The chip application on the site proved to be too light – during the first week there was minimal spare chip left to move around and fall into the gaps left during construction. Even the heaviest application rates were not as heavy as those applied by the Fulton Hogan crew on the Clintons Rd or Telegraph Rd sites. This difference was because the application rates for Motukarara were controlled visually by the chip runner, whereas the Clintons Rd and Telegraph Rd sites were controlled by the chipmaster computer. The chip runner's training to not over-chip prevented him from doing this, even when directed to for a short length.

Table 3.2 Motukarara site layout

Motukarara (State Highway 75) site layout									
		Control (C)	Very very light (VVL)	Very light (VL)	Light (L)	Normal (N)	Heavy (H)	Very heavy (VH)	
→	Left shoulder	□	□	□	□	□	□	□	→
	Left OWP	□	□	□	□	□	□	□	
	Left BWP	□	□	□	□	□	□	□	
Christchurch	Left IWP	□	□	□	□	□	□	□	Akaroa
	Right IWP								
	Right BWP								
←	Right OWP								←
	Right shoulder								

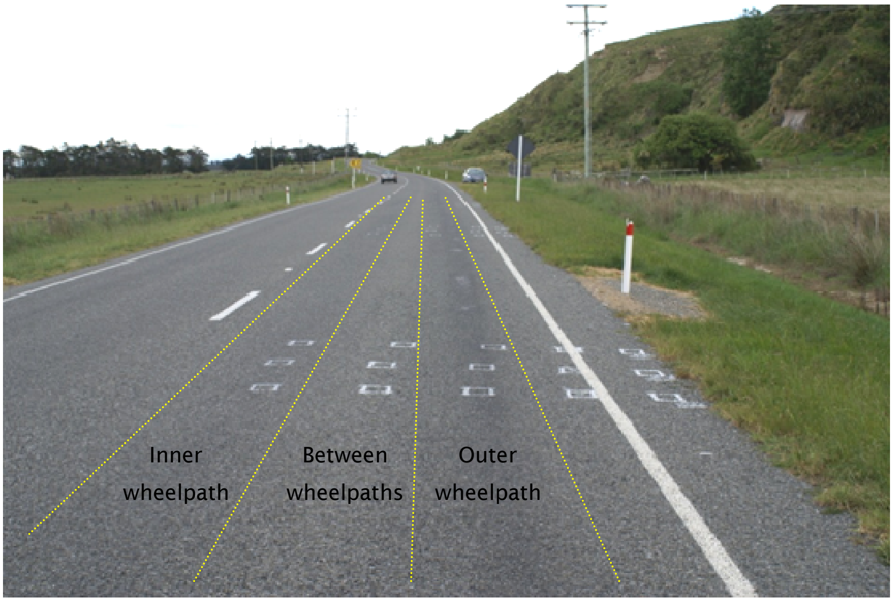
3.3.2.2 Road layout and traffic

The road was a flat, reasonably straight section of State Highway 75, with an average lane width at the site of 3.51m, and an average shoulder width of 0.61m. The site was on the south side of a ridge and was exposed to the cold southerly weather.

The AADT was 2551vpd, with 6.6%HCV. This was the highest-trafficked of the single-coat grade 3 seals in the trial. With much more traffic compacting the seal, the chip locked up quickly, forming a good mosaic where there was enough chip.

As the site was on a reasonably straight section of highway, it provided an overtaking opportunity for motorists, so there was some degree of traffic wander across the road. However, the wheelpaths were quite well defined, as marked in figure 3.5.

Figure 3.5 Motukarara site looking towards Christchurch (4/11/08)



3.3.2.3 Construction

The site was constructed near the end of March, which left little time for the chip to be bedded in before the onset of frosts. The weather was quite settled at time of construction, with no rain during the week after construction.

Monitoring of the seal showed that there was significant movement of chip into and out of the marked frames during the first week after construction. This movement was most likely due to the traffic and then the subsequent sweeping, which would have dislodged and moved the chip into any empty gaps left during construction. The traffic would then have embedded the chip into the binder, which would have still contained some of the solvent and flux.

Most monitoring frames showed a gain of chips during the first week after construction. The amount of increase was controlled by the amount of chip available and the number of gaps left to fill. For example, in the areas with very light application there was a gain in chip numbers, but this was limited because there were fewer loose chips in the vicinity.

3.3.3 Telegraph Rd

3.3.3.1 Chip application

The Pound Rd Quarry sealing chip was applied in one spread across the entire lane, using a Wirtgen self-propelled chipspreader. Unfortunately a sensor had an intermittent fault causing uneven application, with the left-hand side spreading more heavily across the road than the right-hand side. However this didn't affect the longitudinal application rate, which was reasonably consistent for each section.

The telescopic spreader box and good control by the operator meant that there was virtually no double application of chip at the joins.

Figure 3.6 Wirtgen applying chip on the Telegraph Rd site

The Wirtgen operator had a numerical target setting that was used for the chip application on the normal section and subsequently on the control section. Variations of the numerical setting were chosen as the targets for the other application rates and the operator changed to these on the run; the only issue was that it took a relatively large distance before the rate changed through the machine, and this resulted in most of the actual application rates being heavier than the target rates.

Monitoring frames were selected based on the target rates; however, these were generally isolated light areas surrounded by areas with heavier chip application, which provided excess chip that migrated and filled most of the gaps.

Some monitoring frames were selected on the other side of the road, as this area had some patches with the heavy chip application that was not achieved on the same side of the road as the rest of the frames.

The control section was located 100m after the end of the trial section, which allowed the crew to spread the chip at their normal application rate without the pressure of supervision.

Table 3.3 Telegraph Rd site layout

Telegraph Road site layout							
		Very light (VL)	Light (L)	Normal (N)	Heavy (H)	Control (C).	
→	Left shoulder	□	□	□		□	→
	Left OWP	□	□	□		□	
	Left BWP	□	□	□	□	□	
Burnham	Left IWP	□	□	□	□	□	Darfield
	Right IWP						
←	Right BWP						←
	Right OWP				□		
	Right shoulder				□		

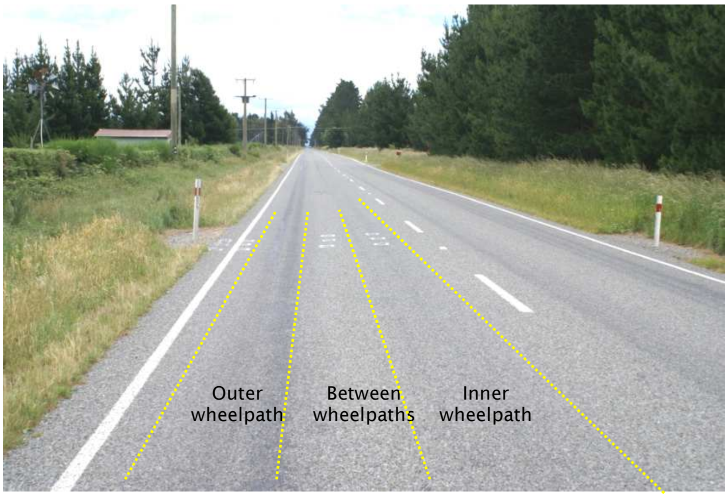
3.3.3.2 Road layout and traffic

The site was a straight, flat section of road with a line of trees on the north side that created shade on the seal in winter. The average lane width on the site was 3.31m, and the average sealed shoulder width outside the edgeline was 0.26m.

The AADT information supplied to us was 646vpd, with 0%HCV. However, after spending time on the site, we estimated that there was at least 5%HCV.

The narrow lane width and shoulder had a channelling effect on the traffic, with most of the HCVs driving on or close to the edgeline, and very little traffic running outside it on the shoulder.

Figure 3.7 Telegraph Rd site looking towards Darfield (16/12/08)



3.3.3.2 Construction

The site was constructed in mid-February and had plenty of time to settle down before the onset of frosts. Issues with the chipspreader during the construction of the seal meant that there was some over-chipping in the lane opposite the site, and traffic and subsequent sweeping moved some of the extra chip onto the monitoring frames.

The weather was reasonably settled and warm in the first few days after construction.

3.3.4 Whitestone Rd

3.3.4.1 Chip application

The Whitestone Rd sealing chip was applied in one spread using an Etnyre Chipmaster chipspreader across the entire lane, edgeline (EL) to CL. The application rate was reasonably consistent on each section, both longitudinally and transversely.

The Etnyre operator had a target setting that he was using for the chip application and we selected various proportions of the target for each section.

The actual monitoring squares were chosen as representative of the section and the application rate that was being targeted.

All test monitoring sites were retained throughout the monitoring period, though grass affected some shoulder sites, and the frames labelled N3 were affected by an agricultural implement scraping chip from the surface.

The control site was chosen after allowing the crew to carry on without interference further along the road, and then selecting a section at random. It received a higher application rate of chip than all of the other sites apart from the section described as ‘very heavy’.

Table 3.4 Whitestone–Five Forks Rd site layout

Whitestone-Five Forks Road site layout								
		Very light (VL)	Light (L)	Normal (N)	Heavy (H)	Very heavy (VH).	Control (C).	
→	Left shoulder	□	□	□	□	□	□	→
	Left OWP	□	□	□	□	□	□	
	Left BWP	□	□	□	□	□	□	
Whitestone	Left IWP	□	□	□	□	□	□	Five Forks
	Right IWP							
	Right BWP							
←	Right OWP							←
	Right shoulder							

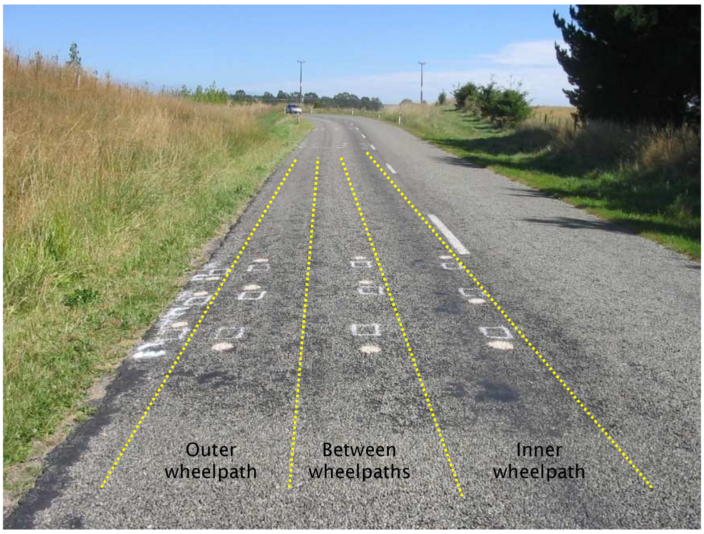
Overall, the chip application on the trial site was rather light, with very little spare chip. This meant that where chip was applied at a 'very light' rate, there was very little spare chip to fill the gaps.

3.3.4.2 Road layout and traffic

The site was flat and mostly straight, with a bend at the end. It was roadmarked with a centreline but no edgelines. The lane width average was 3.2m from the CL to the edge of seal.

The AADT was low, estimated at 250vpd with 5%HCV, so after sweeping there was very little that would dislodge chips, compact chips, or move them about.

Figure 3.8 Whitestone Rd 'light' section looking towards Five Forks (21/1/08)



3.3.4.3 Construction

The site was constructed at the end of March, which left very little time for the chip to be bedded in before the onset of frosts. Monitoring of the seal showed that there was some movement of chip both into and out of the monitoring frames in the trial section during the first week (see appendix C for details). The movement of chip that was recorded was most likely caused by the sweeping of the site, which does move loose chip around and may have introduced some chip from the other side of the road and from downstream of the site. During the first week, most monitoring frames had an increase of chips into the spaces.

Some rain after construction caused some chip loss on other sections of seal that were constructed at the same time as the trial.

3.3.5 Bell Rd

3.3.5.1 Test site layout

The Bell Rd chip was applied using roller spreaders that could not cover the full lane width. This meant it was spread in two runs to cover the lane, resulting in an occasional double-up of chip application in the overlap area.

Figure 3.9 Bell Rd site roller spreader application of the grade 2 chips

Marks were painted on the side of the road and the operator was asked to apply the grade 2 chips at his normal 'racked-in' first chip application rate – this created the control section. Then he was asked to increase the rate for 100m, and then apply it at the 'normal' rate for the next 100m, then apply it at a 'light' rate for the next 100m. The construction direction was towards Napier.

Frames were labelled and photos were taken, and then the second layer, which was grade 4 chip, was applied. The operator was asked to start by applying the grade 4 chip at his 'normal' rate, and then increase the rate to 'heavy' for 50m, then 'light' for 50m, then 'heavy' for 50m, then 'light' for 50m, then 'heavy' for 50m, then 'light' for 50m, to give us the combinations of application rates that we required.

To get a totally random sample for the control, we had to miss taking a photo of the grade 2 chip (the first layer) when it was applied; this meant we could only count the grade 2 chip for the monitoring after construction of the seal, so we did not have an actual count for the initial quantity of grade 2 chip applied.

Table 3.5 Bell Rd site layout

Bell Road (State Highway 2 RS 443/1) site layout

		Light light (LL)	Light heavy (LH)	Normal light (NL)	Normal heavy (NH)	Heavy light (HL)	Heavy heavy (HH)	Control (C)	
	Left shoulder	□	□	□	□	□	□	□	
→	Left OWP	□	□	□	□	□	□	□	→
	Left BWP	□	□	□	□	□	□	□	
Napier	Left IWP	□	□	□	□	□	□	□	Gisborne
	Right IWP								
←	Right BWP								←
	Right OWP								
	Right shoulder								

The chip application was arranged to have the application rates of the grade 2 first chip layer starting 'light' and finishing 'heavy', to avoid having traffic carrying the chip in the direction of travel. However, this should have been done with the grade 4 second coat, as none of the first coat was dislodged and the traffic evened out the second coat application.

3.3.5.2 Road layout and traffic

The site was flat and straight, with a row of poplars on one side and orchard on the other. Shading was not an issue on the test site.

The road was a state highway with a lane width from CL to EL of 3.49m, and a shoulder width from EL to the edge of seal of 0.54m.

This site had the highest traffic level, with an AADT of 5471vpd (including 17.5%HCV), so there was plenty of compaction in the wheelpaths.

3.3.5.3 Construction

The seal was constructed in mid-November, when the weather was warm but changeable, with occasional showers. However, the seal was unaffected by weather.

3.3.6 Mossburn drylock

3.3.6.1 Application

The grade 3 chip was applied using an Etnyre chipmaster chipspreader and the application rates were changed on the run. The target rates were agreed and marked on the shoulder and seal for the Etnyre drivers. They started at the 'light' application rate, increasing through to 'heavy' in the direction of travel, to reduce the risk of the traffic carrying any excess chip from the heavy section onto lighter sections.

After marking the 'light', 'normal' and 'heavy' frames, it was decided there was an opportunity for another set of frames between the 'normal' and 'heavy' sections, so these were marked and called 'normal heavy'. The control section was located 100m further down the road, to ensure that the chip application was unaffected by the trial but still on the same spray length.

Table 3.6 Mossburn drylock site layout

Mossburn drylock (Wreys Bush Mossburn Road) site layout							
		Light (L)	Normal (N)	Normal Heavy (NH)	Heavy (H)	Control (C)	
	Left shoulder	□□□	□□□	□□	□□□	□□	
→	Left OWP	□□□	□□□	□□	□□□	□□	→
	Left BWP	□□□	□□□	□□	□□□	□□	
Wreys Bush	Left IWP	□□□	□□□	□□	□□□	□□	Mossburn
	Right IWP						
←	Right BWP						←
	Right OWP						
	Right shoulder						

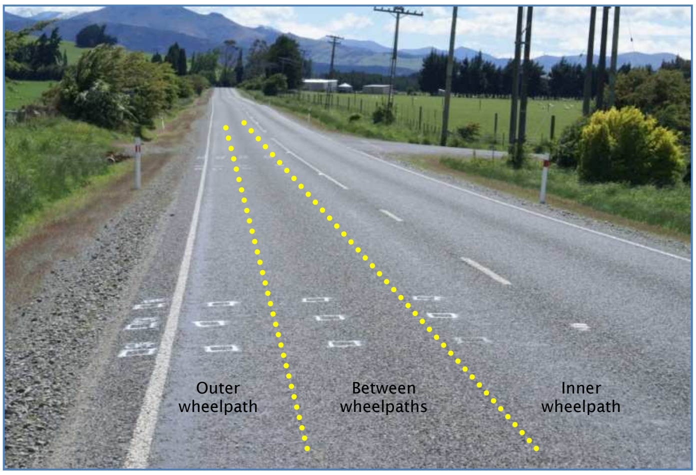
The grade 5 chip was applied using a roller spreader at the normal application rate. Unfortunately, the addition of the grade 5 drylock made it impossible to count the grade 3 chips in some monitoring frames, as some of the larger grade 5 chips were similar in size to the smaller grade 3 chip. The problem was further compounded by some chip breaking down during compaction.

3.3.6.2 Road layout and traffic

The main site was on a slight downhill before a side road, and the control section was opposite a paddock gateway. The site was not affected by shade. The lane width CL to EL averaged 3.0m and the shoulder width EL to the edge of seal averaged 0.35m.

The AADT on the site was 430vpd with 15%HCV; however, there was an increase over the 2006/2007 summer just after construction while transporters carrying windmill parts to the nearby White Hill wind farm travelled over the site. The narrow lane width caused some channelling of the traffic, which caused some binder rise in the wheelpaths.

Figure 3.10 Mossburn drylock site looking west towards Mossburn



3.3.6.3 Construction

The seal was constructed in December and the weather was hot and dry.

Monitoring of the seal showed that the grade 3 chips were locked in place by the grade 5 drylock and there was no grade 3 loss during the first week after construction.

The ‘light’ grade 5 application rate sat down into the gaps between the large chips, so more was retained where the initial grade 3 application rate was light.

There was some aggregate breakdown under the rollers and the traffic and this created uncertainty about the accuracy of the chip counts within the frames, so this was not continued.

3.3.7 Mossburn two-coat seal

3.3.7.1 Chip application

The grade 3 chip was applied using the Etnyre Chipmaster chipspreader, and the grade 5 chip was applied using roller spreaders to maintain productivity.

Three target chip application rates for the grade 3 first chip layer were agreed on and called ‘light’, ‘normal’, and ‘heavy’. The start of each of these sections was marked on the seal and the side of the road (see figure 3.11). It took 10 or 20m for the speed to change on the chipmaster, but once it changed the application rate was reasonably consistent and on target. The sections were constructed so that the site with the ‘light’ application of grade 3 chip first increased to ‘normal’ and then to ‘heavy’ in the direction of the traffic, in case the grade 3 chip moved around.

The grade 5 second chip layer was organised to start with ‘light’ and be followed with ‘heavy’ on each of the grade 3 sections, and this produced sections that were labelled ‘light light’ (short for ‘light first coat grade 3 and light second coat grade 5’). The control section was located away from the research sections, to ensure the application rates were the sealing crew’s normal rates.

Table 3.7 Mossburn two-coat site layout

Mossburn grade 3/5 twocoat (Wreys Bush Mossburn Road) site layout															
		Light light (LL)		Light heavy (LH)		Normal light (NL)		Normal heavy (NH)		Heavy heavy (HH)		Heavy light (HL)		Control (C)	
	Left shoulder	□□□		□□□		□□□		□□□		□□□		□□□		□□	
→	Left OWP	□□□		□□□		□□□		□□□		□□□		□□□		□□	→
	Left BWP	□□□		□□□		□□□		□□□		□□□		□□□		□□	
Wreys Bush	Left IWP	□□□		□□□		□□□		□□□		□□□		□□□		□□	Mossburn
	Right IWP														
	Right BWP														
←	Right OWP														←
	Right shoulder														

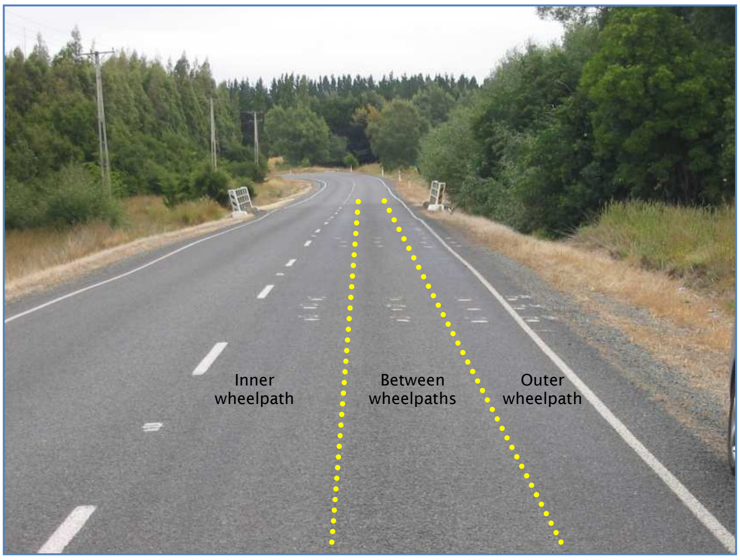
Figure 3.11 Target application rate for grade 3 chip bottom coat

3.3.7.2 Road layout and traffic

The site was on a straight, flat section with a small bridge in the middle; the control section was on a straight, flat section around a bend, separate from the other sections. The lane width CL to EL averaged 3.0m and the shoulder width EL to the edge of seal averaged 0.35m.

The AADT on the site was 430vpd with 15%HCV; however, there was an increase over the 2006/2007 summer just after construction, while transporters carrying windmill parts to White Hill wind farm travelled over the site. The narrow lane width caused some channelling of the traffic, especially at the bridge, and this caused some minor binder rise in the wheelpaths.

Figure 3.12 View southeast on the Mossburn two-coat site



3.3.7.3 Construction

The seal was constructed in early December and the weather was hot and dry.

Monitoring of the seal showed that the grade 3 chips were locked in place by the second spray of binder and application of the grade 5 chip. There was no grade 3 loss throughout the monitoring period.

The 'light' application rate of grade 5 chip sat down into the gaps between the large chips, so more was retained where the initial grade 3 application rate was 'light'.

There was some aggregate breakdown under the rollers and the traffic and this created uncertainty about the accuracy of the chip counts within the frames, so the monitoring was continued but chip counting was discontinued.

4 Seal monitoring methodology

Areas of the target application in each section were chosen and three sets of A5-sized frames were painted on the road on the shoulder (S), outer wheelpath (OWP), between the wheelpath (BWP) and on the inner wheelpath (IWP). These allowed the condition of the seal inside the frames to be compared during the two years after the construction of the seal.

Where possible, photographs of the seal within the frames were taken:

- immediately after construction
- after sweeping
- a month after construction
- before winter
- after winter
- after the next winter.

Each frame was photographed at each visit and where possible, the chips in each frame were compared with those in the previous photograph, to identify the changes – these are documented in appendix C.

Other non-destructive monitoring of the seal inside the frames included counting the chips that had cracked or broken, and estimating the flushed area.

Monitoring tests that affected the chipseal surface were carried out on the chipseal adjacent to each frame, on areas that looked the same as the surface within the frame and were subject to the same trafficking. This included:

- using sand circles to measure the texture depth
- removing chips and estimating binder rise, binder ductility, and binder/seal strength on a qualitative scale.

Each frame on the road was treated as a separate monitoring site, so with seven test locations around the country that had five or more variations of chip application, each with three sets of four painted frames, a total of 484 frames were monitored for the project.

4.1 Chip number monitoring

The chip application monitoring for this project was implemented by taking digital photos of labelled frames and counting the number of chips that had entered the frame/left the frame during the period between each set of photos.

Initially we simply counted the number of chips in the frames, but this was not accurate enough when counting the chips at the margin of the photos, and when the chips broke into pieces. Therefore we repeated the analysis and identified the individual chips that had entered or left the frame by marking each chip that appeared in both photos, and then counting the number of chips gained or lost, as appropriate.

It was often difficult to follow the individual chips in the single-coat seals, because the individual chips in the photos could change shape (visually) as they were reoriented and broke down.

Unfortunately, apart from the initial chip application, the number of chips on the two-coat seal and racked-in seals could not be counted accurately, as the small chip confused the big-stone count and the measure of chip breakdown.

The chip application rates were based on the number of chips applied to the frame. These could be turned into kg/m² if required, as the average weight per chip and the area of the frames were known.

4.2 Effect of traffic

After a newly sealed road has been swept, vehicle tyres interact with the chips and dislodge, reorient, compact, crack or break, and polish them, and this kept the chipseal surfaces in a constant state of flux over the two-year monitoring period. The amount of change caused by the traffic depends mostly on the number of interactions, the type of interactions, the binder properties during the interactions, and the strength of the chip interlock. In this research, the choice of straight, flat sections of road simplified this somewhat, as the traffic passing over them needed to do little braking, turning or accelerating.

The number of interactions was quantified for some sections and estimated for others based on the traffic data supplied. Most traffic tends to travel in a similar transverse location on the road (wheelpaths), generally between the edgeline and centreline markings. This means there will be more interactions in the wheelpaths than on the less-trafficked shoulders, and between the wheelpaths.

Xaioduan and Tekell (2005) reported that the lateral displacement of traffic on rural roads at tangent (straight) sites showed that 68% of traffic ran 0.3–0.6m off the centreline, 11% of traffic ran on the centreline, 19% ran within 0.3–0.6m of the edgeline, and 2% ran on or beside the edgeline. For the purposes of this research, these values have been extrapolated to mean 68% of traffic runs in the wheelpaths, 19% runs between the wheelpaths, and 2% runs on the shoulders.

The chipsealing industry recognises the value of the traffic in compacting and forming the stone mosaic in chipseal, and once the seal is swept and roadmarked, the traffic normally becomes channelised so that the expected number of interactions in the transverse locations is as described above.

From the discussions above we could expect that with more tyre–stone interactions, there should be more chip loss in the wheelpaths than at other locations. However, these interactions help form the chip layer into a tightly compacted stone mosaic, and the binder has the appropriate properties to allow chip reorientation and movement without breaking the bond. This normally occurs in summer.

On low-trafficked roads or transverse locations (ie shoulder) where there are not enough tyre–stone interactions to adequately form a tightly compacted stone mosaic before the end of summer, the chips are more susceptible to being dislodged and chip loss can result. However because there is less traffic, there is less interaction that can dislodge the chip.

4.3 Binder chip interface

An important factor in the formation of the chipseal is the reorientation of the chip towards the ALD vertical position, and compaction or embedment into the binder by the traffic. The following properties of the sealing binder are important in this interaction:

- binder viscosity at surface temperature during construction and trafficking
- binder adhesiveness at surface temperature during construction and trafficking
- binder adhesiveness, cohesiveness and ductility after sweeping.

The binder's viscosity has to be low enough to allow the chip to be embedded into it, and to reorient in it once embedded. This is usually managed by the use of cutback (traditionally kerosene) in the binder. Some of the kerosene can stay in the binder for 12 months or more, and this allows the chip to be embedded into, and move around in, the binder during this period.

Houghton (1987) suggested that 'The lowering of binder viscosity by the addition of kerosene to a sealing binder not only affects chip wetting but increases the rate of initial compaction …' and concluded that the percentage of voids in the seal filled with binder at the beginning of winter is '… significantly affected by the initial viscosity of the reseal binder …'

The cutback and adhesion agent improve the adhesiveness (stickiness) of the binder, especially in the first few weeks. This enables the binder to adhere to chips that are dislodged or reoriented when they land on the binder.

Sealing is generally carried out in summer to make use of the warmth, which lowers the viscosity and enhances the adhesiveness of the binder. Once the weather cools, the binder stiffens up, which inhibits the reattachment of chips. At some of the trial sites, the surface temperatures could get down to well below 0°C, and possibly some down to -15°C – at these temperatures the binder becomes very stiff and if the chip is dislodged, the binder may fail, resulting in chip loss.

The binders used on the trial sites in the South Island all contained automotive gas oil (AGO, sometimes called diesel), which is a longer-term softening agent (see appendix B). This may have allowed some of the loose chip to adhere even up to 20 months after construction.

4.4 Seal construction timing

As discussed above, the compaction and reorientation of the chips into a tight stone mosaic relies on the number of tyre and chip interactions and the binder properties. Both of these are affected by the timing of the seal construction; there have to be enough tyre–chip interactions during the summer months, when the surface temperature is warm, to form the mosaic and embed the chips before the cold temperatures stiffen up the binder.

In his conclusions, Houghton (1987) suggested that: '… there is a minimum % of binder filled voids required at the beginning of the first winter …'. The inference is that seals constructed late in the season do not have time for the chip to be reoriented and fully embedded before the temperatures cool. Also, where the chips are over-applied, the chips can be trapped in the average greatest dimension (AGD) vertical position, which produces higher void volume in the chips and means that the chip–binder interface will be reduced. It would be expected that areas with over-chipping in seals constructed late in the season would lose more chip than areas with under-chipping in seals constructed late in the season.

4.5 Seal monitoring data analysis

For completeness, monitoring was carried out on most facets of the chipseal properties. However, there were only four of these that were likely to be affected by the chip application rate, and the comparison of performance versus the actual chip application was analysed for each of the following:

- chip application rate and change
- texture change
- binder rise
- chip breakdown.

Other properties that were monitored included binder strength and binder ductility. As the same binders were used for each site, they did not vary from section to section – the monitoring showed that they were consistent from section to section with each visit, and had no relationship with the four facets analysed in full. Therefore the results for these were not included in the appendices.

Flushing was only recorded on very isolated spots and was obviously related to the previous surface, so this was not analysed further and the results were not included in the appendices.

5 Chip application analysis

5.1 Chip mobility

Data tables in appendix C show the changes in the monitoring frames, with chips gained and chips lost during each monitoring period.

The data in the tables shows that on some seals and various chip application rates, a significant number of chips moved around after they were applied, both during and after sweeping on single-coat seals, and long after construction.

The most significant chip movement was caused by the sweeping – the loose chip was moved from areas where it had been over-applied and deposited into the voids left where chip had been under-applied.

The amount of loose chip on the site was affected by the chip application rate applied outside the trial sections. Where the normal application rate resulted in excess chip, there was a large number of loose chips; but where the normal application rate resulted in very little excess, there were very few loose chips.

On sites where there were significant quantities of excess chip being swept over the monitoring frames, the trial application rates were basically reset.

In practice, the chip application is normally consistent – it may be high or low, but the application rate depends on the supervisor’s visual target. When the target is high there are a lot of loose chips but few voids for them to fall into, and when the target is low there are few loose chips to fit into the many voids.

The monitoring showed that chips that were identified as having moved into the voids generally stayed in place, but were more likely to shift again than those that were initially applied and compacted into the binder.

As chip that is rolling around on the chipseal surface is more susceptible to being crushed by traffic, the chips that move to fill the voids are generally smaller than the initial chip size and fit more easily into the surface voids of the chipseal.

5.2 Effect of chip application rate

It was assumed that chip mobility would be greater in areas with excessively high or low application rates, for the following reasons:

- Where the chip was over-applied it would be trapped with its AGD vertical, with less surface area in contact with the binder, and could be more easily levered out by tyre contact. Also, any excess chip on top of other chip would not be attached to the binder. In both cases chips could be easily dislodged and mobilised by traffic.
- Where the chip was under-applied it would have a much higher surface area in contact with the binder and less height, so would present less leverage for tyres to dislodge it. However, the chips would be more isolated and would not be supported by surrounding chip, and this could allow the traffic to roll or dislodge them.

However, the data shows that the issue of chip mobility is much more complex than we envisaged, and it includes many other factors such as chip shape, traffic counts, HCV counts, transverse location of the traffic, traffic speed, road geometry, chip availability, binder application rate, binder viscosity, date of construction, and road surface aspect.

5.3 Texture monitoring

Texture monitoring was carried out adjacent to each of the monitoring frames, taking care not to test any area that had been affected by previous testing. On some sites where there was residue sand left from the previous testing, the sand circle testing was completed adjacent to the previous test patches on areas that looked similar in texture and level of retained chip.

Figure 5.1 Motukarara C2 shoulder and OWP monitoring frames and sand circles

The main aim of this project was to investigate the effect that the chip application rate had on the long-term performance of the chipseal – the surface texture of the chipseal in the monitoring frames was a good indication of the effect of the chip application rates. The change in the surface texture from ‘after sweeping’ to ‘final monitoring’ of the seal adjacent to the frame was compared to the chip application rate in the frame (after sweeping) for the four transverse locations on each of the trial sites.

5.4 Analysis of texture versus chip application rate

The change in texture and the final measured texture have been graphed against the number of chips applied for each of the sites and each of the four transverse locations on the road.

A summary of the comparison data is provided in appendix D.

5.4.1 Single-coat seal texture loss versus chip application rate

Only 8 out of the 16 locations showed any relationship, with 6 of these showing increasing texture loss with increasing chip application rate, and 2 showing decreasing texture loss with increasing chip application rate.

5.4.2 Single-coat seal final texture versus chip application rate

Only 7 out of the 16 locations showed a relationship between the texture at the end of monitoring and the chip application rate. Of these, 4 showed increasing texture with increasing chip application rate, and 3 showed decreasing texture with increasing chip application rate.

5.4.3 Drylock seal texture loss versus chip application rate

Only 3 out of 8 locations showed a relationship, with 2 showing a decrease in texture loss with increasing chip application rate, and the other showing an increase in texture loss with increasing chip application rate.

5.4.4 Drylock seal final texture versus chip application rate

Only 1 out of 8 locations showed a weak relationship of increasing texture with increasing chip application rate. None of the other 7 locations showed any relationship between the final texture and the initial chip application rate.

5.4.5 Two-coat seal texture loss versus chip application rate

All 4 locations showed a weak-to-average relationship, with 3 showing decreasing texture loss with increasing chip application rate, and the other showing an increase in texture loss with increasing chip application rate.

5.4.6 Two-coat seal final texture versus chip application rate

All 4 locations showed a weak or good relationship between final texture and chip application rate, with 3 out of 4 locations showing increasing final texture with increasing chip application rate.

5.4.7 Discussion

There was very little consistency in the data, which suggests that chip application rates are not the main influence on the long-term texture of a chipseal.

The 4 single-coat chipseals showed no consistency between seals or locations, suggesting that the chip application rate was not a factor in the rate of chip loss and the texture depth achieved at the end of monitoring.

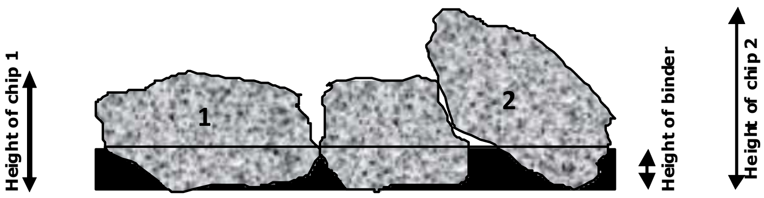
The only two-coat (Mossburn two-coat) chipseal monitored for this project showed that in the trafficked areas, a heavier application of the first layer of chip resulted in greater texture, and slower texture loss, over the monitoring period. However a heavier application of the first layer of chip also resulted in less texture, and faster texture loss, on the less-trafficked shoulder.

The results for the 2 drylock chipseals monitored in this trial were somewhat consistent with the two-coat results.

5.5 Binder rise monitoring

Monitoring of the binder rise was carried out by removing chips from the seal in line with, but outside, each of the monitoring frames. The assessment was based on the proportion of the chip's height that the binder had reached. The height of the chip was based on the orientation it had in the road, with the assumption that the binder line was the horizontal – see figure 5.2, where the proportion of the binder rise up chip 1, which is lying flat with ALD vertical, is much higher (33%) than that for chip 2, which is not lying flat (20%).

Figure 5.2 Binder rise assessment diagram



The assessment was made by removing five chips at random and calculating an average of the binder rise for the five chips, and selecting one of the categories in appendix A (Seal condition rating system) under 'binder rise' or 'no binder rise'. The initial range for the 'binder rise' (which was based on an Australian seal assessment tool) was set too high, so the additional 'no binder rise' categories were added to ensure that the binder rise could be categorised accurately.

5.5.1 Discussion

The analysis of the effect of the chip application rate on the binder rise during the monitoring period is in appendix E.

In summary, there was no obvious relationship between chip application rates and binder rise.

There were obvious differences where the binder rise was generally greater in the wheelpaths than between the wheelpaths and the shoulders.

Where there were isolated areas with existing flushing or excess binder that were not treated before sealing, these reflected through and caused flushing in the new seals within two years after sealing.

5.6 Chip breakdown

Monitoring of chip breakdown was carried out at each monitoring visit by visually assessing each monitoring frame for each section. It was a difficult and rather inaccurate method, as only the obvious cracked or broken chips were counted. Those chips where a piece had fallen off were not always identified, and those chips that had crushed and disintegrated could only be identified if remnants were left behind.

A second measurement was made counting broken and cracked chips on the monitoring photos – this was compared with the field counts, and showed some variance with the site assessments.

5.6.1 Discussion

The analysis of the comparison of the chip breakdown versus the amount of chip applied using both methods of assessment is in appendix F.

The data shows that variation in chip application rates did not have a measureable effect on the amount of chip breakdown in the first two years after the chipseals' construction.

Unfortunately it was almost impossible to identify chips that were broken on the Bell Rd and Mossburn two-coat, because the application of the second coat of chip disguised what was happening in the chipseal.

It was expected that there would be more breakdown where the chip application was heavier. However, on the single-coat seals great care had been taken to only apply the various application rates with a single layer of chip, with very little chip sitting on top of each other, and this probably reduced the amount of chip-on-chip crushing by tyres.

This research found no relationship between the chip application rate and the amount of chip breakdown after the first two years of the seals' life.

6 Project summary

- Seven chipseals were constructed with varied chip application rates, and the effect of the different chip application rates on the performance of the seals was monitored.
- The sites had a range of traffic loadings, but were generally straight and flat.
- The range of chip application rates on most sites included ‘very light’ to ‘very heavy’.
- The different chip application scenarios (frames) monitored totalled 484 and provided a significant amount of data.
- The monitoring of these frames showed that the chip application rate did not directly affect chipseal performance in the first two years after construction.
- Traffic volumes and traffic distribution had a significant effect on texture change, binder rise and chip breakdown.
- The existing surface condition also had a significant effect on the amount of texture change, binder rise and flushing.

Amongst experienced practitioners, the general consensus on chip application is that a complete stone mosaic is the optimum, and it is better to apply extra chip than to leave gaps in the mosaic. This has resulted in a general tendency for the industry to over-apply chip by an estimated 10%, to make sure there are no gaps in the stone mosaic.

- This research has shown that under-applying chip on low-stress sites does not reduce the performance of chipseals in the first two years after construction.
- It is proposed that on low-stress sites, the target chip application rate should be reduced so that the aim is to apply the exact amount required, with no wastage of chip.

6.1 Conclusions

- Millions of dollars is wasted every year because excess chip is used during the construction of chipseals. Extra costs include the cost of the chip, transport costs, sweeping costs and windscreen repair costs.
- Experts in New Zealand and around the world cannot agree on chip application rates, how to measure them, and how to specify them.
- Chip application rates that are generally higher than required are targeted by both contractors and site engineers to ensure there are enough loose chips on the chipseal surface to complete the chip mosaic during trafficking. The high chip application rates have been identified as wasteful and adding cost, so the industry should agree to target lower chip application rates than the current practice.
- The New Zealand chipsealing industry needs a specification that includes actual chip application rate targets in New Zealand, and an accepted method or tool to accurately measure the application rate.
- Incomplete chip coverage does not cause early chipseal failure in the low-stress environment.
- Two years was insufficient time to measure the effect of the chip application rates on chipseal lives.

7 Recommendations

- On low-stress sites, the target chip application rate should be reduced so that the aim is to apply the exact amount required, with no wastage of chip.
- A chip application specification for New Zealand, and an accepted method or tool to enable the practitioners to comply with it, should be developed.
- Further investigation should be carried out on chipseals subjected to higher traffic volumes and higher stress, to ascertain what effect the chip application rate has on their performance.

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Appendix A: Seal condition rating system

A1 Aggregate breakdown

No breakdown = 0

Isolated single chips crushed <1% = 1

1%< crushed chips <5% = 3

>5% crushed chips = 5

>20% crushed chips = aggregate failure

Note: Need scores for S, OWP, BWP, and IWP.

A1.1 Aggregate loss – calculated from photo chip counts

Closely packed and uniformly distributed = 0

Single isolated aggregate loss <1% = 1

1%< single, isolated pockets of aggregate loss <5% = 3

5%< widespread pockets of aggregate loss <30% = 5

Aggregate loss >30% = seal failure

Note: Need scores for S, OWP, BWP, and IWP.

A1.2 Surface texture depth (from representative sand circles)

T_D >2.5mm = 0

1.5mm < T_D <2.5mm = 1

1.1mm < T_D <1.5mm = 3

0.9mm < T_D <1.1mm = 5

T_D <0.9mm = seal failure

Note: Need scores for S, OWP, BWP, and IWP.

A1.3 Binder rise

Binder $\leq \frac{2}{3}$ up chip = 0

$\frac{3}{4}$> binder up chip > $\frac{2}{3}$ = 1

$^{9}/_{10}$> binder up chip > $\frac{3}{4}$ = 3

Binder > $^{9}/_{10}$ up chip = 5

Binder over chip = seal failure

Note: Need scores for S, OWP, BWP, and IWP.

A1.4 No binder rise

Binder ≤⅔ up chip = 0

½> binder up chip >⅓ = 1

⅓> binder up chip >¼ = 3

Binder <¼ up chip = 5

Minimal binder on chip = seal failure if chip loss

Note: Need scores for S, OWP, BWP, and IWP.

A1.5 Binder strength (record binder temperature)

Chips pop out after some effort (some chips break when trying to remove) = 0

Chips difficult to remove (need a screwdriver to lever out) = 1

Chips reasonably easy to remove (can pop out with key) = 3

Chips easy to remove (can roll out with finger) = 5

Note: Need scores for S, OWP, BWP, and IWP.

A1.6 Binder ductility (length of tail)

Extreme ductility (>200mm) = 0

Medium ductility (51–200mm) = 1

Minimal ductility (10–50mm) = 3

Nil or low ductility (<10mm) = 5

Note: Need scores for S, OWP, BWP, and IWP.

A1.7 Bleeding/flushing

No bleeding or flushing = 0

<5% bleeding or flushing = 1

5% < bleeding or flushing <10% = 3

>10% bleeding or flushing = 5

>30% bleeding or flushing = seal failure

Note: Need scores for S, OWP, BWP, and IWP.

The assessment should be carried out at these times:

- high-temperature performance – January–February each year
- low-temperature performance – between September and November each year.

A2 Procedure for measuring

A2.1 Chip application and chip loss

Digital photos should be taken of marked frames of the seal, for reference. The assessor/s should carry out an objective assessment on site.

A2.2 Binder rise

Chips should be removed from each transverse location, and the level of binder up the chip assessed and agreed on by the assessors.

A2.3 Binder strength

The strength of the binder should be assessed when removing chips for the binder rise assessment.

A2.4 Binder ductility

The ductility of the binder should be assessed when removing chips for the binder rise assessment.

A2.5 Surface texture depth

Sand circles should be taken at S, OWP, BWP and IWP, beside the frames.

Figure A1 Sand circling at the Motukarara site

Appendix B: Chipseal design information

Table B1 Chipseal design information

	Location description	Traffic counts	Chip source	Chip ALD	Average chip mass	Date sealed	Binder recipe grade AGO/Kero/AA	Kinematic viscosity @ 60℃ (cSt)	Design method	Design binder application rate	Actual binder application rate
Bell Road site	SH2 / 443 / 1 ends at the intersection with Bell Road	5471 17.5% HCV (TNZ 2006)	Poplar Lane	10.82mm 6.92mm	4.00g 1.11g	16/11/2006	80/100 0/7/0.7	44400	Fulton Hogan	2.40l/m²	2.41l/m²
Motukarara site	SH 75 / 24 / 1.99 starts at the intersection with Seabridge Road	2551 6.6% HCV (TNZ 2006)	McLeans Island	9.00mm	2.27g	23/03/2007	180/200 1/3/0.7	17400	Isaac Construction	2.06l/m²	2.06l/m²
Clintons Road site	Clintons Road between Ridgens and Milton Roads	126 vpd O% HCV (SDC 2006)	Pound Road	9.28mm	2.34g	8/02/2007	180/200 1/4/0.8	16500	Fulton Hogan	2.80l/m²	2.80l/m²
Telegraph Road site	Telegraph Road between Clintons and Courtenay Roads	646 vpd O% HCV (SDC 2006)	Pound Road	9.42mm	2.39g	13/02/2007	180/200 1/4/0.8	16900	Fulton Hogan	2.70l/m²	2.70l/m²
Mossburn grade 3	Wreys Bush Mossburn road near Hamlyn Road intersection	430 vpd 15% HCV (SDC 2006)	Wreys Bush	9.28mm	2.86g	6/12/2006	180/200 2/3/0.8	16300	Fulton Hogan	2.25l/m²	2.22l/m²
Mossburn two coat	Wreys Bush Mossburn Road near Hamlyn Road intersection	430 vpd 15% HCV (SDC 2006)	Wreys Bush	9.28mm 4.55mm	2.86g	6/12/2006	180/200 2/3/0.8	16300	Fulton Hogan	1.00l/m² 1.00l/m²	1.01l/m² 1.01l/m²
Whitestone Road	Whitestone Five Forks Road between Burnside and Enstone Road	Not supplied Est 250vpd	Oamaru Shingle	9.09mm	2.50g	28/03/2007	180/200 2/3/0.7	16000	Lindsay Roundhill	2.90l/m²	2.89l/m²

Appendix C: Chip change

C1 Clintons Rd chip change (constructed 8/2/07)

Table C1 Clintons Rd chip application monitoring data

Clinton Road chip application monitoring data													
	8/02/2007	13/02/2007		12/03/2007		13/07/2007		5/03/2008		16/12/2008		16/12/2008	
	Chip applied	Gained	Lost	Gained	Lost	Gained	Lost	Gained	Lost	Gained	Lost	Chip retained	Chip change
Shoulder													
VVL1	154	1	1	0	0	11	1	2	9	8	3	162	8
VL2	169	18	5	4	12	1	1	2	4	8	2	178	9
VVL2	169	1	5	0	1	6	6	12	18	10	0	168	-1
VL3	175	19	1	6	13	3	9	6	3	3	4	182	7
C1	176	8	2	1	0	9	2	3	8	8	1	192	16
VVL3	176	6	2	0	2	5	5	3	4	9	0	186	10
L1	180	3	3	0	0	8	3			8	10	183	3
L2	181	0	2	0	3	7	3			12	15	177	-4
C3	185	6	0	1	1	3	4	1	1	8	1	197	12
VL1	187	14	1	0	3	5	9	5	3	2	1	196	9
C2	198	4	5	0	0	5	5	4	6	5	1	199	1
L3	204	3	7	1	1	12	14			3	19	182	-22
VH3	208	13	11	1	4	4	14	2	3	2	1	197	-11
H2	213	10	12	3	2	5	3	3	1	3	0	219	6
N1	218	7	6	4	0	1	8	2	6	1	2	211	-7
N3	219	6	3	2	4	3	4	1	3	7	5	219	0
H1	220	11	14	1	1	2	3	3	3	4	1	219	-1
N2	222	7	5	1	4	4	7	2	3	4	1	220	-2
VH2	227	7	12	1	1	3	7	0	2	2	0	218	-9
VH1	237	8	7	3	11	1	4	2	2	3	1	229	-8
H3	244	4	12	1	2	1	0	2	1	4	2	239	-5
Outer wheelpath													
VVL2	135	45	0	0	2	3	9	2	2	8	1	179	44
VVL3	146	35	0	1	0	0	7	2	4	5	1	177	31
VVL1	168	30	0	0	2	4	9	5	3	7	1	199	31
L1	173	1	2	1	0	4	10			12	7	172	-1
L2	174	6	0	0	0	2	7			9	4	180	6
VL2	174	4	2	2	0	2	3	1	3	3	1	177	3
VL3	176	13	3	1	0	0	4	1	0	3	0	187	11
C2	178	4	3	0	0	7	3	3	2	4	2	186	8
VL1	181	8	4	1	1	3	5	1	0	6	0	190	9
L3	198	1	1	4	0	1	6			5	4	198	0
C1	201	4	1	0	0	1	1	3	1	3	2	207	6
N3	201	12	5	1	3	1	5	0	1	4	1	204	3
C3	204	8	1	0	0	1	4	2	0	6	0	216	12
N1	204	4	2	0	1	5	6	2	3	0	3	200	-4
N2	206	8	2	0	0	1	5	2	1	6	2	213	7
H1	224	12	5	1	1	2	8	1	0	3	0	229	5
H2	233	3	6	2	0	1	2	1	1	2	0	233	0
VH3	233	9	13	0	0	0	4	0	0	1	3	223	-10
VH1	234	3	7	0	0	1	4	0	0	2	1	228	-6
VH2	246	5	8	0	1	0	5	1	0	1	2	237	-9
H3	247	9	7	1	1	0	3	1	1	3	0	249	2
Between wheelpaths													
VVL2	138	42	0	0	0	2	4	2	1	0	0	179	41
VVL3	142	39	1	0	0	8	5	3	5	9	2	188	46
VL2	163	10	5	1	0	2	5	1	1	0	2	164	1
VVL1	167	31	1	1	0	2	10	4	2	4	4	192	25
VL1	179	9	3	1	1	5	2	4	2	2	3	189	10
VL3	179	17	0	1	0	4	6	1	3	2	2	193	14
L2	203	9	3	0	0	6	13			1	1	202	-1
L3	210	10	0	1	0	6	12			3	7	211	1
C3	215	13	7	1	1	1	3	2	0	3	0	224	9
N1	219	9	5	1	0	1	3	0	2	1	0	221	2
N3	223	17	6	2	1	2	12	0	2	2	4	221	-2
N2	225	29	5	1	0	4	3	0	0	3	6	248	23
L1	226	21	13	1	0	7	3			4	2	241	15
C1	230	21	21	2	1	3	1	0	0	1	0	234	4
C2	239	17	11	0	0	0	1	0	0	0	1	243	4
H2	242	22	9	2	1	1	0	0	0	1	0	258	16
H3	249	13	12	2	0	0	1	0	0	0	0	251	2
VH1	259	10	29	1	2	3	5	3	3	5	0	242	-17
VH3	259	10	13	2	2	0	0	3	3	1	0	257	-2
H1	268	19	12	0	1	2	6	0	0	0	0	270	2
VH2	268	16	17	0	0	0	1	0	0	2	0	268	0
Inner wheelpaths													
VVL1	103	13	0	2	1	0	0	2	1	2	0	120	17
VVL2	128	6	0	2	1	0	2	0	0	0	0	133	5
L2	134	9	1	1	0	3	2			2	2	144	10
VL2	140	10	0	1	0	2	0	2	2	3	0	156	16
VVL3	149	1	0	0	0	0	1	3	0	2	1	153	4
VL1	150	15	0	4	0	2	2	3	2	7	1	176	26
L3	159	9	0	1	0	2	5			3	3	166	7
L1	160	5	1	3	1	2	6			3	4	161	1
H2	162	4	0	1	0	1	3	1	1	0	0	165	3
C3	164	8	2	2	1	1	2	0	1	0	1	168	4
N1	176	14	0	0	0	0	3	1	0	0	1	187	11
N2	179	8	1	0	0	2	4	1	1	4	0	188	9
H3	180	4	3	0	1	0	1	3	0	4	0	186	6
N3	180	29	1	1	0	1	2	0	2	1	0	207	27
H1	181	2	1	1	0	4	0	2	2	1	2	186	5
C2	184	2	1	1	0	0	0	1	0	0	0	187	3
C1	200	11	3	0	1	1	0	1	0	1	0	210	10
VL3	201	12	1	2	2	3	4	2	4	1	1	209	8
VH1	209	11	3	0	0	0	2	1	0	10	1	225	16
VH2	217	8	7	2	0	0	1	0	1	0	0	218	1
VH3	229	15	7	0	2	1	1	0	0	5	1	239	10

C1.1 After 1 week (13/2/07)

One week after construction there had been a lot of chip movement, with an average of 11.4 chips gained and 4.7 chips lost.

The high binder application rate and the level of solvent in the binder had combined to ensure that the chips stuck to the binder when they fell into gaps and touched it hours (or even days) after construction. The softness of the binder had also allowed chips that were not well stuck to be dislodged and moved around by the sweeping and by traffic.

C1.2 After 5 weeks (12/3/07)

The amount of chip moving about had declined significantly, averaging 1.1 chips gained and 1.1 chips lost from the monitoring frames.

The reduction of chip movement was expected – as the chip formed a mosaic and became locked in place, more of the solvent had evaporated out and the binder had stiffened. Also, there was little traffic to dislodge or move chip around.

C1.3 After 5 months (13/7/07)

The arrival of the first frosts in autumn brought colder ground temperatures that had further stiffened the binder. The traffic had dislodged some chip, usually more from the low-trafficked areas.

The monitoring frames averaged 2.6 chips gained and 4.3 chips lost. The shoulder frames had more change, gaining an average of 4.7 chips and losing an average of 5.3 chips.

Because of the road shape, the normal direction of movement of chip when flicked by a car tyre was out of the wheelpaths towards the edge of the seal.

Even though there was chip loss in the colder weather, probably due to cohesive failure, a number of chips were gained after they landed in gaps in the chip layer and stuck to the binder.

C1.4 After 13 months (5/3/08)

After the spring and summer months, the amount of chip being moved around had slowed to an average of 1.8 chips gained and 2.0 chips lost from each monitoring frame.

There was an average of 3.1 chips gained and 4.4 chips lost from the shoulder monitoring frames, more than twice the amount moving in the other locations. The lack of traffic on the shoulder would have contributed to this loss rate, as there would be less compaction by trafficking. The higher gain rate was likely to be because chips tend to be flicked from the wheelpaths to the side of the road, and some of these would have found spaces to fill on the shoulder.

C1.5 After 22 months (16/12/08)

The amount of chip change had further increased, to an average of 3.6 chips gained and 1.9 chips lost. The amount of change was higher in the shoulder and OWP monitoring frames than in the BWP and IWP frames.

C1.6 Summary – from construction (8/2/07) to 22 months (16/12/08)

C1.6.1 Shoulders (S)

In this period, 10 monitoring frames lost chip overall, 1 frame had no change, and 10 frames had an increase overall.

The largest amount of change in the 22 months after construction was 38.3%. This occurred on the shoulder in the third frame in the ‘very light’ section (VL3). This frame had a 21.1% gain and 17.1% loss – ie a 4.0% loss of chip in a frame that had had the fourth-lowest chip application rate on the shoulder at construction.

The next-largest change in the 22 months after construction was 34.9%, with 17.2% gained and 17.8% lost – ie a total change of -0.6% in a frame that had had the third-lowest initial chip application rate.

C1.6.2 Outer wheelpath (OWP)

Five frames lost chip overall, 2 frames had no change, and 14 frames showed an increase in chips over the 22 months after construction.

The largest amount of change was 53.3%. This occurred on the OWP in the second frame in the ‘very very light’ section (VVL2). This frame had a 43.0% gain and 10.4% loss – ie a net change of 32.6% increase, which was the largest for the OWP frames. The VVL2 had had the lowest initial application rate of the OWP frames.

The next-largest change was 37.7%. This occurred on the OWP in the third frame in the ‘very, very light’ section (VVL3). This frame had a 29.9% gain and 8.2% loss of chip during the 22 months of monitoring after construction – ie a net gain of 21.2%.

C1.6.3 Between wheelpaths (BWP)

Four frames lost chip overall, 1 frame had no change, and 16 frames showed gain in chip after 22 months of monitoring.

The amount of change was 50.7% (VVL3), with 41.5% chips gained and 9.2% chips lost – ie a net gain of 32.4%, the largest net change for the BWP frames. VVL3 had had the second-lowest initial chip application rate for the BWP frames.

The next-largest change was 37.0% (VVL2) with 33.3% chips gained and 3.6% chips lost – ie a net gain of 29.7%. VVL2 had had the lowest initial chip application rate for the BWP frames.

C1.6.4 Inner wheelpath (IWP)

All 21 IWP frames had a net gain of chips during the 22 months of monitoring after construction.

The largest amount of change was 24.0%. This occurred on the IWP in the second frame in the ‘very light’ section (VL1). This frame had a 20.7% gain and 3.3% loss of chips – ie a net gain of 17.3%, the largest net change for the IWP frames. VL1 had had the sixth-lowest initial chip application rate for the IWP frames.

The next-largest amount of change was 20.6%. This occurred on the IWP in the third frame in the normal section (N3). This frame had a 17.8% gain and 2.8% loss of chips – ie a net gain of 15.0%. N3 had had the fourteenth-lightest initial chip application rate for the IWP frames.

C2 Motukarara chip change (constructed 23/3/2007)

Table C2 Motukarara chip application monitoring data

Note: Shaded cells indicate extrapolated numbers

Motukarara chip application monitoring data											
	23/03/2007	2/04/2007		8/06/2007		28/02/2008		4/11/2008		4/11/2008	
	Chip applied	Gained	Lost	Gained	Lost	Gained	Lost	Gained	Lost	Chip retained	Chip change
Shoulder											
VVL3	112	4	3	2	1	9	2	0	4	117	5
VVL1	121	2	0	1	0	9	2	1	1	131	10
VL3	131	4	0	0	0	8	5	6	5	139	8
L1	142	12	0	0	1	5	0	3	0	161	19
VL1	146	7	1	1	1	9	3	2	0	160	14
VVL2	155	4	0	1	0	1	5	0	1	155	0
VL2	157	4	2	1	0	8	2	2	9	159	2
L2	181	8	2	1	1	5	1	8	0	199	18
L3	182	11	2	0	0	8	1	3	1	200	18
C2	204	26	6	1	1	2	1	4	0	229	25
N1	208	9	4	2	4	5	5	1	0	212	4
VH2	209	16	9	2	1	3	5	2	0	217	8
C3	211	22	11	1	5	1	0	5	1	223	12
H1	212	10	0	2	1	3	3	0	1	222	10
VH1	214	20	2	3	6	6	0	3	1	237	23
N2	216	9	7	1	2	6	2	1	0	222	6
VH3	220	4	2	7	14	6	4	6	0	223	3
C1	224	26	12	1	0	1	3	2	0	239	15
H3	227	7	8	1	3	5	1	3	0	231	4
N3	227	17	11	0	2	3	2	0	0	232	5
H2	230	8	16	1	1	4	0	1	0	227	-3
Outer wheelpath											
VVL2	116	5	0	1	0	1	5	0	0	118	2
VL3	131	3	1	0	1	5	7	0	2	128	-3
VL1	135	3	0	1	1	2	4	0	0	136	1
VVL3	141	3	0	1	0	1	7	0	1	138	-3
VL2	142	10	0	0	0	1	5	1	4	145	3
VVL1	146	5	2	1	0	0	1	0	1	148	2
L1	175	15	1	0	2	1	4	1	3	182	7
L2	189	8	1	0	2	0	1	0	1	192	3
L3	191	11	3	0	1	0	12	1	0	187	-4
H2	195	31	0	0	0	0	0	0	0	226	31
N3	199	15	2	0	0	0	0	0	0	212	13
N2	201	10	2	2	0	1	2	1	0	211	10
N1	205	12	1	0	0	0	0	0	0	216	11
H3	211	20	3	0	1	0	0	0	0	227	16
C1	216	20	1	0	0	0	0	0	0	235	19
C2	224	16	3	0	0	0	1	0	0	236	12
VH2	229	37	1	0	0	1	3	2	1	264	35
C3	232	22	2	0	0	0	0	0	0	252	20
VH1	249	1	4	1	14	0	3	0	1	229	-20
VH3	249	6	0	0	1	1	4	0	0	251	2
H1	253	23	0	0	0	0	0	0	0	276	23
Between wheelpaths											
VL1	97	8	0	0	0	1	1	0	0	105	8
VVL1	112	9	1	0	1	0	4	0	0	115	3
VVL2	116	6	0	0	0	0	1	0	0	121	5
VVL3	119	4	0	0	1	0	6	0	0	116	-3
VL2	120	20	0	2	6	0	1	0	0	135	15
VL3	129	4	0	0	0	2	3	0	1	131	2
N3	149	13	2	0	0	1	0	0	0	161	12
N1	154	26	0	0	0	1	0	0	1	180	26
H3	156	37	1	0	0	0	3	0	1	188	32
N2	155	24	0	0	0	0	1	0	0	178	23
L1	163	20	1	0	0	1	0	1	0	184	21
L3	164	26	5	0	0	1	1	1	0	186	22
H2	171	50	2	0	4	1	0	0	1	215	44
H1	189	45	1	0	3	0	1	0	0	229	40
L2	198	22	2	1	1	1	0	0	0	219	21
VH1	205	22	5	0	1	1	0	0	0	222	17
VH2	205	27	7	0	1	0	4	0	0	220	15
VH3	212	46	9	0	0	2	3	1	1	248	36
C3	231	26	6	0	0	0	0	0	0	251	20
C2	232	26	7	0	1	0	0	0	0	250	18
C1	226	10	2	0	1	1	0	0	0	234	8
Inner wheelpath											
L2	154	26	2	0	0	3	1	2	0	182	28
L1	157	25	2	1	0	0	0	0	0	181	24
H1	166	20		2	2	2	0	2	0	190	24
N3	172	15		0	0	1	0	2	0	190	18
VVL1	174	14	1	0	0	0	1	1	0	187	13
H2	174	15		0	0	3	0	0	0	192	18
VL3	178	24	4	0	1	0	0	0	0	197	19
VL2	179	23	2	1	0	0	1	1	0	201	22
L3	180	15	1	1	0	1	0	0	0	196	16
VVL2	180	20	7	0	0	0	0	0	0	193	13
H3	182	12		2	0	1	0	0	0	197	15
C3	183	37	5	0	0	0	0	0	0	215	32
N1	185	12		0	0	2	0	0	0	199	14
C2	187	29	4	0	0	1	6	0	1	206	19
N2	188	12		0	0	1	0	2	1	202	14
VH1	189	12		1	4	1	2	0	1	196	7
VVL3	192	12	9	0	0	1	0	0	0	196	4
VL1	196	10	0	0	0	0	0	0	0	206	10
C1	203	19	9	0	0	0	0	0	0	213	10
VH2	206	10		1	0	0	0	0	0	217	11
VH3	210	10		0	3	0	2	0	0	215	5

C2.1 After 1 week (2/4/07)

A large amount of chip had moved into and out of the monitoring frames during the first week. It was expected that a high level of chip would be retained in the first week, as the binder contained 3pph (parts per hundred) of kerosene, which made the binder sticky even at ambient temperatures.

The overall average was 16.0 chips gained and 3.0 chips lost. The BWP frames gained an average of 22.4 and lost an average of 2.4. The gains came from the chip application overlap near the IWP, and other spare chips from outside of the test site.

C2.2 After 9 weeks (8/6/07)

There was very little change at this point, suggesting the stone mosaic had formed and the binder had stiffened up, holding the chip in place. There were average gains of 0.6 chips and losses of 1.2 chips per monitoring frame on the entire site. The weather was reasonably settled during this time.

The traffic probably re-orientated most of the chip during this time frame, forming a solid chip mosaic.

C2.3 After 11 months (28/2/08)

The winter months and some extreme frosts and cold snaps had hardened the binder, contributing to the chip loss and allowing some chip movement. The average gains per monitoring frame for the site were 1.8 chips, and the average losses were 1.8 chips. There were more losses than gains from the IWP, BWP and OWP, and more gains than losses on the shoulder because the chip that was dislodged from the lane migrated to the shoulder.

C2.4 After 20 months (4/11/08)

There was very little change in most of the monitoring frames, with an average of 0.9 chips gained and 0.6 chips lost. The monitoring frames on the shoulder gained an average of 2.5 chips, and lost an average of 1.1 chips.

C2.5 Summary – from construction (23/3/07) to 20 months (4/11/08)

C.2.5.1 Shoulder (S)

Most shoulder monitoring frames (19/21) showed an increase in chips during the monitoring period, 1 showed no change, and 1 showed a small (1.3%) decrease.

The average change for the 21 monitoring frames on the shoulder was 10.8% in gains and 5.3% in losses – ie a net gain of 5.5% overall.

The largest amount of change (22.3%) was in VVL3, where there was 13.4% gain and 8.9% loss – ie a net gain of 4.5%. This frame had had the lowest initial chip application rate.

The next-largest amount of change (21.4%) was in VL3, where there was 13.7% gain and 7.6% loss – ie a net gain of 6.1%. This frame had had the third-lowest initial chip application rate.

The largest net gain was in L1 (13.4%, from 14.1% gain and 0.7% loss). This frame had had the fourth-lowest chip application rate.

C.2.5.2 Outer wheelpath (OWP)

During the monitoring period, most OWP monitoring frames (17/21) showed a gain of chips, and 4 showed a loss of chip.

The average total change for the 21 monitoring frames was 10.7%, with 7.4% in gains and 3.3% in losses – ie a net gain of 4.1% overall for the OWP frames.

The largest total change (19.7%) was in frame VH2, with 17.5% gain (the largest in the OWP frames) and 2.2% losses – ie a net gain of 15.3%. This frame had had the fifth-highest chip application rate out of the OWP frames.

The next-largest total change (15.9%) was in frame H2, with 15.9% gain and 0.0% loss – ie a net gain of 15.9%, the highest net gain of the OWP frames. This frame had had the tenth-lowest initial chip application rate out of the OWP frames.

C.2.5.3 Between wheelpaths (BWP)

Most BWP monitoring frames (20/21) had an overall gain in chips during the monitoring period, and 1 had a loss.

The average total change for the 21 BWP monitoring frames was 16.6%, with an average of 13.6% gains and 3.0% losses – ie an average net gain of 10.6%.

The largest total change (33.9%) was in frame H2, with 29.8% gains and 4.1% losses – ie a net gain of 25.7%. This frame had the largest gain and the largest net gain out of the BWP monitoring frames.

The next-largest total change (29.2%) was in frame VH3, with 23.1% gains and 6.1% losses – ie a net gain of 17.0% chips.

C.2.5.4 Inner wheelpaths (IWP)

Nine of the frames had to be shifted, as 3 sections were located too wide and 9 OWP frames were painted over with the edgeline (see figure C1). To solve this problem, the original 9 BWP frames became OWP, the original 9 IWP frames became BWP, and 9 new IWP frames had to be established a week after construction. Unfortunately this meant there were no original photos of the initial chip application rate for these 9 new frames, so this was estimated.

Figure C1 Roadmarking paint obscuring a frame – photo taken 2 April 2007

All 21 of the IWP monitoring frames showed an overall gain in chips during the 20-month monitoring period.

The average total change for the 21 IWP monitoring frames was 12.7%, with an average of 10.9% gains and 1.9% losses – ie producing an average net gain of 9.0% for the IWP frames.

The largest total change (23.0%) was in frame C3, with 20.2% gains and 2.7% losses – ie a net gain of 17.5%. This frame also had the largest gain of the IWP frames.

The next-largest total change (22.1%) was in frame L2, with 20.1% gains and 1.9% losses – ie a net gain of 18.2%, the largest net gain in the IWP frames.

C3 Telegraph Rd chip change (constructed 13/2/2007)

Table C3 Telegraph Rd chip application monitoring data

Telegraph Road chip application monitoring data											
	13/02/2007	12/03/2007		13/07/2007		5/03/2008		16/12/2008		16/12/2008	
	Chip applied	Gained	Lost	Gained	Lost	Gained	Lost	Gained	Lost	Chip retained	Chip change
Shoulder											
C3	210	12	7	2	4	2	5	1	2	209	-1
VL3	212	11	13	1	4	0	1	0	0	206	-6
VL1	213	16	3	0	2	0	0	0	0	224	11
C1	219	27	25	8	14	4	14	0	1	204	-15
L2	224	21	11	7	22	8	13	6	9	211	-13
VL2	226	12	18	0	3	0	0	0	0	217	-9
H3	227	16	0	1	8	0	1	1	2	234	7
C2	232	12	20	4	4	1	7	0	0	218	-14
L3	236	21	15	7	17	3	14	4	6	219	-17
N2	244	3	5	13	14	3	10	3	4	233	-11
N3	245	4	19	10	8	1	11	4	7	219	-26
L1	248	10	29	7	12	3	12	2	5	212	-36
H1	249	7	15	6	6	2	3	0	1	239	-10
N1	249	2	10	6	11	0	5	6	3	234	-15
H2	258	0	1	0	1	0	5	0	1	250	-8
Outer wheelpath											
N3	199	55	0	0	5	1	0	0	0	250	51
VL1	200	18	7	0	1	1	2	1	0	210	10
N2	209	60	0	0	1	0	0	0	1	267	58
L1	215	21	6	0	0	0	0	0	1	229	14
VL3	219	15	3	0	0	0	0	0	0	231	12
N1	228	45	0	0	0	0	0	0	0	273	45
L2	232	18	5	0	0	0	0	0	0	245	13
C2	236	10	4	0	1	1	1	1	0	242	6
H1	237	7	0	0	0	0	1	0	0	243	6
VL2	248	21	5	0	0	0	0	0	0	264	16
H3	252	0	23	0	0	0	0	0	0	229	-23
H2	255	0	13	0	0	0	1	0	0	241	-14
L3	256	21	7	0	0	0	0	0	0	270	14
C1	259	2	14	1	1	0	0	0	0	247	-12
C3	262	6	9	0	0	0	1	0	0	258	-4
Between wheelpaths											
VL3	162	31	2	0	1	0	0	0	0	190	28
VL2	163	23	1	0	0	0	0	0	0	185	22
L1	172	25	4	0	0	0	0	0	1	192	20
VL1	174	16	5	1	0	1	0	0	0	187	13
L2	190	20	4	0	0	0	0	0	0	206	16
N2	196	41	7	0	0	0	0	0	0	230	34
L3	198	23	8	0	1	0	0	0	0	212	14
N3	205	17	5	0	0	0	1	0	0	216	11
H3	207	43	0	0	1	0	0	0	0	249	42
C1	212	26	1	0	1	0	1	0	0	235	23
H2	214	45	0	0	2	1	1	0	0	257	43
H1	220	35	3	0	1	0	0	0	0	251	31
C3	224	21	9	0	0	0	1	0	0	235	11
C2	225	13	4	0	0	0	0	0	0	234	9
N1	230	24	7	0	0	0	0	0	0	247	17
Inner wheelpath											
VL2	159	21	2	0	0	0	0	0	0	178	19
L1	163	27	0	0	1	0	1	0	0	188	25
VL1	176	7	0	0	1	1	0	0	0	183	7
L3	178	22	1	0	0	0	0	0	0	199	21
N3	180	41	1	0	0	0	0	0	0	220	40
C2	181	18	1	1	0	0	0	0	0	199	18
C1	182	15	1	0	0	1	0	0	0	197	15
VL3	190	13	3	0	0	0	0	0	0	200	10
N1	192	37	1	0	0	0	0	0	0	228	36
L2	201	20	4	0	0	0	0	0	0	217	16
C3	206	14	2	1	0	0	0	0	0	219	13
N2	215	32	1	0	0	0	0	0	0	246	31
H2	229	20	0	0	3	1	0	0	1	246	17
H1	244	0	7	0	1	1	0	0	0	237	-7
H3	247	1	8	0	1	1	0	0	0	240	-7

C3.1 After 1 month (12/3/07)

There had been some chip movement in the monitoring frames during the first month, with an average of 19.4 chips gained and 6.3 chips lost. It is thought that most of this change happened in the week after construction and when the site was swept.

The binder application rate had been high and it contained both AGO and kerosene, so any chips that touched the binder were very likely to become attached to it.

C3.2 After 5 months (13/7/07)

By this point, the chip movement had decreased to an average of 1.3 chips gained and 2.6 chips lost. This reduction was due to the chip forming a stone mosaic and the binder hardening, and also there was less loose chip in the area. Most of the chip movement occurred in the shoulder frames, where there was an average of 4.8 chips gained and 8.7 chips lost.

When they are dislodged by a vehicle, chips tend to roll outwards to the shoulder, down the crossfall. Because the traffic tends not to run on the shoulders outside the edgeline, the seal on the shoulder does not get a lot of compaction, and this means it is susceptible to chip loss when traffic does pass over it.

C3.3 After 12 months (5/3/08)

Chip movement had decreased even further, with an average of 0.6 chips gained and 1.9 chips lost. The seal had settled down, with very few loose chips apart from those that ended up on the shoulder, which had an average gain of 1.8 chips and loss of 6.7 chips.

C3.4 After 21 months (16/12/08)

There had been very little chip movement on the seal, with an average of 0.5 chips gained and 0.8 chips lost. The shoulder had an average gain of 1.8 chips and loss of 2.7 chips.

C3.5 Summary – from construction 13/2/07 to 21 months 16/12/08

C3.5.1 Shoulder (S)

In this period, 13 out of 15 frames on the shoulder lost chips and 2 gained chips.

The largest amount of chip movement was 43.3% (L2), with 18.8% gained and 24.6% lost – ie a 5.8% loss for the period. L2 had had the sixth-lowest initial chip application rate in the shoulder frames.

The next-largest chip movement was 42.5% (C1), with 17.8% gained and 24.7% lost – ie a 6.9% loss for the period. C1 had had the fourth-lowest initial chip application rate in the shoulder frames.

The largest chip change was 14.5% loss from L1, which had had the twelfth-highest initial chip application rate.

C3.5.2 Outer wheelpath (OWP)

During the 21 months after construction, 4 out of 15 frames in the OWP lost chips, and the other 11 frames gained chips.

The largest amount of chip movement was 30.7% (N3), with 28.1% gained and 2.5% lost – ie a 25.6% gain for the period. N3 had had the lowest initial chip application rate in the OWP frames.

The next-largest chip movement was 29.7% (N2), with 28.7% gained and 1% lost – ie a 27.7% gain for the period, which was the largest chip change for the OWP frames. N2 had had the third-lowest initial chip application rate in the OWP frames.

C3.5.3 Between wheelpaths (BWP)

All 15 BWP frames gained chips during the 21 months after construction.

The largest amount of chip movement was 24.5% (N2), with 20.9% gained and 3.6% lost – ie a 17.3% gain for the period. N2 had had the sixth-lowest initial chip application rate in the BWP.

The next-largest amount of chip movement was 22.9% (H2), with 21.5% gained and 1.4% lost – ie a 20.1% gain for the period. H2 had had the eleventh-highest initial chip application rate in the BWP frames.

The largest chip change was 20.3% (H3) gain in the frame that had had the ninth-highest initial chip application rate in the BWP frames.

C3.5.4 Inner wheelpath (IWP)

During the 21 months after construction, 2 out of the 15 IWP frames lost chips (those that had had the highest initial chip application rate at the IWP) and the other 13 frames gained chips.

The largest amount of chip movement was 23.3% (N3), with 22.8% gained and 0.6% lost – ie a 22.2% gain, the highest for the IWP over the monitoring period. N3 had had the fifth-lowest initial chip application rate in the IWP frames.

The next-largest amount of chip movement was 19.8% (N1), with 19.3% gained and 0.5% lost – ie an 18.8% gain.

C4 Whitestone Rd chip change (constructed 28/3/2007)

Table C4 Whitestone Rd chip application monitoring data

Whitestone Road chip application monitoring data											
	28/03/2007	4/04/2007		22/05/2007		21/01/2008		25/11/2008		25/11/2008	
	Chips applied	Gained	Lost	Gained	Lost	Gained	Lost	Gained	Lost	Chips retained	Chip change
Shoulder											
L1	106	0	1	0	0	0	1	0	0	108	2
L2	119	1	0	1	2	1	2	2	2	130	11
VL2	135	6	0	2	1	2	8	2	5	161	26
VL1	138	4	1	0	2	0	8	5	0	158	20
H1	141	1	0	0	0	0	7	0	1	150	9
L3	141	1	1	1	2	2	3	0	0	151	10
VL3	141	4	3	1	3	1	1	1	1	156	15
H2	143	2	1	1	0	0	4	0	1	152	9
N2	145	1	0	0	0	1	1	0	0	148	3
N3	152	1	0	1	1	0	1	2	1	159	7
VH1	157	4	0	1	2	2	4	0	1	171	14
H3	163	1	2	0	0	0	0	0	0	166	3
N1	166	0	1	0	0	0	11	2	1	181	15
C3	171	3	3	1	2	1	2	0	2	185	14
C1	172	3	3	5	0	0	3	0	0	186	14
VH3	172	3	1	0	0	0	2	0	1	179	7
VH2	187	3	2	0	1	0	2	0	2	197	10
C2	196	11	6	0	0	0	12	0	1	226	30
Outer wheelpath											
L1	119	4	0	1	5	0	7	1	0	137	18
L2	121	1	2	0	1	0	2	0	0	127	6
N3	130	3	2	0	0	0	2	0	0	137	7
L3	135	1	1	0	2	0	1	0	0	140	5
N1	142	0	0	0	0	0	2	1	0	145	3
H1	149	2	1	0	0	0	3	0	1	156	7
VL1	151	7	1	1	1	0	3	0	0	164	13
VL3	156	7	1	0	3	1	2	0	2	172	16
N2	163	1	3	1	0	0	1	1	0	170	7
C1	168	1	3	0	0	0	0	0	0	172	4
C2	171	4	2	0	2	1	0	0	0	180	9
H2	172	1	2	0	1	0	1	0	0	177	5
VL2	174	6	3	0	0	0	1	0	0	184	10
VH3	179	6	5	0	0	1	0	0	0	191	12
C3	182	5	4	0	0	1	0	0	0	192	10
H3	190	4	3	0	2	0	5	0	0	204	14
VH2	196	1	8	0	0	0	0	0	0	205	9
VH1	228	0	11	0	0	0	0	0	0	239	11
Between wheelpaths											
L2	120	4	2	0	2	1	1	0	12	142	22
VL1	123	6	4	0	2	1	6	1	0	143	20
N1	125	2	3	0	0	0	3	2	0	135	10
L1	130	2	3	1	0	1	2	2	2	143	13
L3	130	2	2	1	2	2	1	3	2	145	15
VL2	142	6	4	0	0	5	1	1	0	159	17
VL3	152	5	3	0	0	3	2	0	1	166	14
VH2	153	4	3	1	1	1	2	0	0	165	12
N2	154	1	0	0	0	0	2	1	2	160	6
H3	159	10	1	0	0	1	0	3	18	192	33
VH3	165	9	4	0	0	1	3	0	3	185	20
H2	167	7	6	0	0	1	0	1	0	182	15
VH1	171	7	4	0	1	1	2	1	2	189	18
N3	172	7	6	0	0	0	1	0	1	187	15
H1	177	5	3	1	0	2	3	1	0	192	15
C2	184	6	5	1	1	3	7	0	0	207	23
C1	198	5	11	0	0	0	5	0	2	221	23
C3	202	11	11	0	2	0	2	0	0	228	26
Inner wheelpath											
L2	113	0	0	1	0	0	3	0	2	119	6
VL1	118	7	0	1	0	0	4	1	0	131	13
VL2	129	10	1	2	0	2	6	0	0	150	21
L3	130	2	2	0	0	1	2	1	0	138	8
L1	131	3	1	0	0	0	1	0	0	136	5
VL3	131	3	0	0	3	1	10	0	1	149	18
N2	135	0	0	0	0	0	0	2	0	137	2
H2	143	3	0	0	0	0	0	0	0	146	3
H1	147	0	0	1	0	1	1	0	0	150	3
N1	152	2	1	0	0	0	0	1	0	156	4
N3	161	1	1	0	0	0	0	1	0	164	3
H3	162	3	1	0	0	1	1	0	0	168	6
VH1	162	2	1	0	1	0	3	0	0	169	7
C3	171	5	2	0	0	0	4	0	0	182	11
C1	179	4	0	0	1	1	2	0	0	187	8
C2	187	1	4	0	0	0	1	0	0	193	6
VH2	189	3	3	0	0	0	1	0	0	196	7
VH3	194	2	2	0	0	1	0	2	0	201	7

C4.1 After 1 week (4/4/07)

At the end of the first week after construction there had been some chip movement, as at the other sites, with an average of 3.5 chips gained and 2.4 chips lost.

The amount of chip moving about and sticking was expected, as the binder contained 3pph of kerosene, which made it sticky and allowed the chip to attach to the binder even after it had cooled to ambient temperatures.

C4.2 After 7 weeks (22/5/07)

At this point, the number of chips moving into and out of the marked frames had decreased significantly, with 0.4 chips gained and 0.8 chips lost. This was expected, as more kerosene had evaporated from the binder and the road temperature had cooled, so the binder was stiffer, holding the chip in place, though not so cold that the binder had become brittle.

C4.3 After 10 months (21/1/08)

The amount of chip change had increased to an average of 0.6 chips gained and 2.6 chips lost. Most of the chip lost was from the shoulder, which had an average of 0.6 chips gained and 4.0 chips lost.

The chip loss was probably the result of chip being dislodged by traffic while the binder was hard in the winter, as evidenced by holes in the binder film. There were also indications that some chip may have been rolled over while the binder was soft, especially in the areas with a light chip application rate, where there was less support from adjacent chips.

C4.4 After 20 months (25/11/08)

The amount of chip movement had slowed a little to an average of 0.6 chips gained and 1.0 chip lost. The most change had occurred BWP, with 0.9 chips gained and 2.5 chips lost.

It seems that the most damage to the seal had been done by the small amount of traffic that ran over these frames during winter.

C4.5 Summary – from construction (28/3/07) to 20 months (25/11/08)

C4.5.1 Shoulders (S)

At the end of the monitoring period, most marked frames (15/18) had a loss of chip, 2 had a small gain, and 1 had no change.

The largest amount of change in the 20 months after construction was 19.3% (VL2), with 8.9% chip gained and 10.4% lost. This had had the third-lowest initial chip application rate. Overall, VL2 had less than 2% loss.

The next-largest change was 15.3% (C2), with 5.6% chip gained and 9.7% lost, at the site with the highest initial application rate. However, C2 had a 4.1% loss of chip overall.

There was no relationship between the amount of chip applied and the amount of chip lost

C4.5.2 Outer wheelpath

At the end of monitoring, most marked frames (12/18) had a loss of chip, 5 had a gain of chip, and 1 had no change.

The largest amount of change in the 20 months after construction was 15.1% (N1), with 5.0% chip gained and 10.1% lost, at the site of the lowest initial application rate. N1 had a 5.0% loss of chip overall.

The next-largest change was 10.3% (VL3), with 5.1% chip gained and 5.1% lost. VL3 had no change overall.

There was no relationship between the amount of chip applied and the amount of chip lost.

C4.5.3 Between wheelpaths

At the end of monitoring, most marked frames (10/18) had a loss of chip, 5 had a gain of chip, and 3 had no change.

The largest amount of change in the 20 months after construction was 20.8% (H3), with 8.8% chip gained and 11.9% lost at the site with the lowest initial application rate. H3 had a 3.1% loss of chip overall.

The next-largest change was 18.3% (VL3), with 4.2% chip gained and 14.2% lost. VL3 had a 10% loss of chip overall.

There was no relationship between the amount of chip applied and the amount of chip lost.

C4.5.4 Inner wheelpath

At the end of monitoring, most marked frames (11/18) had a gain of chip, 6 had a loss of chip, and 1 had no change.

The largest amount of change in the 20 months after construction was 16.3% (VL2), with 10.9% chip gained and 5.4% lost, at the site with the lowest initial chip application rate. VL2 had a 5.4% gain of chip overall.

The next-largest change was 13.7% (VL3), with 3.1% chip gained and 10.7% chip lost. VL3 had a 7.6% loss of chip overall.

There was no relationship between the amount of chip applied and the amount of chip lost.

Because the inner wheelpath was closest to the centreline, and therefore closer to the more heavily applied chip on the other side of the road, the extra chip that had landed in the inner wheelpath spaces had then been compacted by the traffic.

C5 Bell Rd chip change (constructed 16/11/2006)

Table C5 Bell Rd chip application monitoring data

Bell Road chip application monitoring data		
	Frame Label	Grade 2 Chip Applied
Shoulder		
Control (C)	C1	86
Heavy Heavy (HH)	HH1	126
	HH2	119
Heavy Light (HL)	HL1	135
	HL2	132
Normal Heavy (NH)	NH1	114
	NH2	95
Normal Light (NL)	NL1	118
	NL2	114
Light Heavy (LH)	LH1	80
	LH2	88
Light Light (LL)	LL1	86
	LL2	80
Outer wheelpath		
Control (C)	C1	141
Heavy Heavy (HH)	HH1	134
	HH2	138
Heavy Light (HL)	HL1	142
	HL2	129
Normal Heavy (NH)	NH1	119
	NH2	120
Normal Light (NL)	NL1	119
	NL2	109
Light Heavy (LH)	LH1	106
	LH2	93
Light Light (LL)	LL1	80
	LL2	91
Between wheelpaths		
Control (C)	C1	100
Heavy Heavy (HH)	HH1	121
	HH2	141
Heavy Light (HL)	HL1	124
	HL2	129
Normal Heavy (NH)	NH1	106
	NH2	102
Normal Light (NL)	NL1	94
	NL2	102
Light Heavy (LH)	LH1	82
	LH2	83
Light Light (LL)	LL1	88
	LL2	80
Inner wheelpath		
Control (C)	C1	106
Heavy Heavy (HH)	HH1	138
	HH2	123
Heavy Light (HL)	HL1	139
	HL2	126
Normal Heavy (NH)	NH1	96
	NH2	97
Normal Light (NL)	NL1	102
	NL2	99
Light Heavy (LH)	LH1	88
	LH2	96
Light Light (LL)	LL1	75
	LL2	65

It proved to be too difficult to count the grade 2 chips after covering them with the grade 4 second coat, so the chip-change monitoring on this site was restricted to general observations, as follows:

- The frames that had had the initial heavy application of grade 2 chip lost more of the second layer of chip over time than those that had had light and normal initial applications.
- There was no grade 2 chip loss from any of the monitoring frames during the monitoring period.

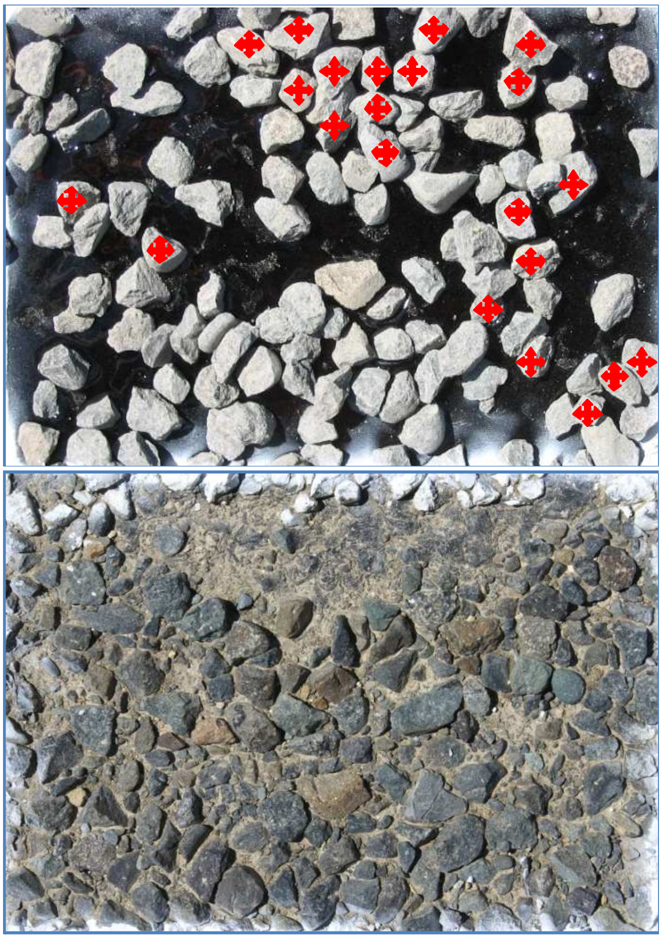
C6 Mossburn drylock chip change (constructed 6/12/2006)

Table C6 Mossburn drylock chip monitoring data

Mossburn drylock chip monitoring data		
Grade 3 bottom coat	Frame label	6/12/2006 Chip applied
Shoulder		
Control	C1	127
	C2	152
Heavy	H1	127
	H2	147
	H3	116
Light	L1	118
	L2	100
	L3	85
Normal	N1	109
	N2	115
	N3	111
Normal-heavy	NH1	138
	NH2	129
Outer wheelpath		
Control	C1	132
	C2	153
Heavy	H1	170
	H2	165
	H3	142
Light	L1	113
	L2	138
	L3	113
Normal	N1	143
	N2	164
	N3	156
Normal-heavy	NH1	134
	NH2	149
Between wheelpaths		
Control	C1	142
	C2	133
Heavy	H1	166
	H2	166
	H3	177
Light	L1	156
	L2	127
	L3	135
Normal	N1	124
	N2	141
	N3	151
Normal-heavy	NH1	155
	NH2	155
Inner wheelpath		
Control	C1	135
	C2	164
Heavy	H1	170
	H2	166
	H3	154
Light	L1	148
	L2	143
	L3	106
Normal	N1	138
	N2	149
	N3	135
Normal-heavy	NH1	145
	NH2	159

The monitoring of the frames included counting the gaps left by chips that were lost. A reasonable amount of chip was lost from most of the frames located along the shoulder. The worst location was N1S, which lost an estimated 22 chips during the monitoring period (see figure C2). The only other recorded loss of grade 3 chips was from both N1BWP and N2BWP.

Figure C2 Top – N1S grade 3, 6 December 2006 (22 chips lost); bottom – N1S grade 3/5 drylock 26 November 2008



As discussed earlier, the application of the grade 5 drylocking coat made it virtually impossible to distinguish between grade 5 chip that was applied, broken grade 3 chip, and chips that had been gained from elsewhere.

Unfortunately this meant that the chip change within the frames could not be accurately monitored, so it was not reported.

C7 Mossburn two-coat data (constructed 6/12/2006)

Table C7 Mossburn two-coat chip application data

Mossburn two-coat chip application data 6/12/2006		
Bottom coat grade 3		Number of chips applied
Shoulder		
Control	C1	93
	C2	94
Heavy grade 3 Heavy grade 5	HH1	106
	HH2	97
	HH3	111
Heavy grade 3 Light grade 5	HL1	134
	HL2	125
	HL3	129
Light grade 3 Heavy grade 5	LH1	108
	LH2	80
	LH3	78
Light grade 3 Light grade 5	LL1	71
	LL2	71
	LL3	85
Normal grade 3 Heavy grade 5	NH1	97
	NH2	78
	NH3	80
Normal grade 3 Heavy grade 5	NL1	90
	NL2	93
	NL3	69
OWP		
Control	C1	93
	C2	91
Heavy grade 3 Heavy grade 5	HH1	143
	HH2	128
	HH3	101
Heavy grade 3 Light grade 5	HL1	151
	HL2	163
	HL3	156
Light grade 3 Heavy grade 5	LH1	112
	LH2	107
	LH3	107
Light grade 3 Light grade 5	LL1	93
	LL2	85
	LL3	107
Normal grade 3 Heavy grade 5	NH1	124
	NH2	77
	NH3	113
Normal grade 3 Heavy grade 5	NL1	116
	NL2	105
	NL3	114
BWP		
Control	C1	95
	C2	89
Heavy grade 3 Heavy grade 5	HH1	137
	HH2	139
	HH3	141
Heavy grade 3 Light grade 5	HL1	156
	HL2	146
	HL3	169
Light grade 3 Heavy grade 5	LH1	154
	LH2	86
	LH3	92
Light grade 3 Light grade 5	LL1	82
	LL2	112
	LL3	94
Normal grade 3 Heavy grade 5	NH1	95
	NH2	94
	NH3	103
Normal grade 3 Light grade 5	NL1	117
	NL2	94
	NL3	94

Mossburn two-coat chip application data 6/12/2006		
Bottom coat grade 3		**Number of chips applied**
IWP		
Control	C1	97
	C2	102
Heavy grade 3 Heavy grade 5	HH1	141
	HH2	141
	HH3	132
Heavy grade 3 Light grade 5	HL1	154
	HL2	168
	HL3	174
Light grade 3 Heavy grade 5	LH1	118
	LH2	117
	LH3	92
Light grade 3 Light grade 5	LL1	75
	LL2	102
	LL3	95
Normal grade 3 Heavy grade 5	NH1	105
	NH2	108
	NH3	121
Normal grade 3 Heavy grade 5	NL1	119
	NL2	118
	NL3	115

As with the drylock and racked-in seals, the second coat of chip in the two-coat chipseal made it impossible to accurately count the chips in the monitoring frames. From visual assessment of the frames, it appeared that there was no loss of the grade 3 chips during the monitoring period.

Appendix D: Texture vs chip application rate

Table D1 Summary comparing texture with increasing chip application rates

Site	Texture loss 16/12/08 R^2	Comment	Texture depth 16/12/08 R^2	Comment
Clintons Rd				
Shoulder	0.47	Average, incr	0.50	Average, decr
OWP	0.24	Weak, incr	0.06	Nil
BWP	0.34	Average, incr	0.24	Weak, incr
IWP	0.00	Nil	0.03	Nil
Motukarara				
Shoulder	0.03	Nil	0.04	Nil
OWP	0.04	Nil	0.18	Weak, decr
BWP	0.01	Nil	0.09	Nil
IWP	0.03	Nil	0.06	Nil
Telegraph Rd				
Shoulder	0.02	Nil	0.45	Average, incr
OWP	0.17	Weak, decr	0.31	Average, incr
BWP	0.46	Average, incr	0.20	Weak, decr
IWP	0.19	Weak, incr	0.00	Nil
Whitestone Rd				
Shoulder	0.15	Weak, incr	0.05	Nil
OWP	0.06	Nil	0.08	Nil
BWP	0.11	Weak, decr	0.13	Weak, incr
IWP	0.04	Nil	0.04	Nil
Bell Rd				
Shoulder	0.02	Nil	0.08	Nil
OWP	0.10	Nil	0.04	Nil
BWP	0.20	Weak, decr	0.07	Nil
IWP	0.21	Weak, decr	0.07	Nil
Mossburn drylock				
Shoulder	0.20	Weak, incr	0.01	Nil
OWP	0.00	Nil	0.00	Nil
BWP	0.03	Nil	0.03	Nil
IWP	0.00	Nil	0.11	Weak, incr
Mossburn two-coat				
Shoulder	0.17	Weak, incr	0.18	Weak, decr
OWP	0.15	Weak, decr	0.45	Average, incr
BWP	0.34	Average, decr	0.36	Average, Incr
IWP	0.18	Weak, decr	0.56	Good, incr

Coefficient of determination (R^2):

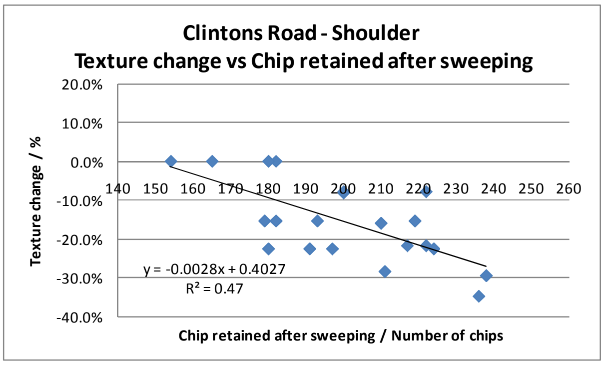
≤0.10 Nil relationship

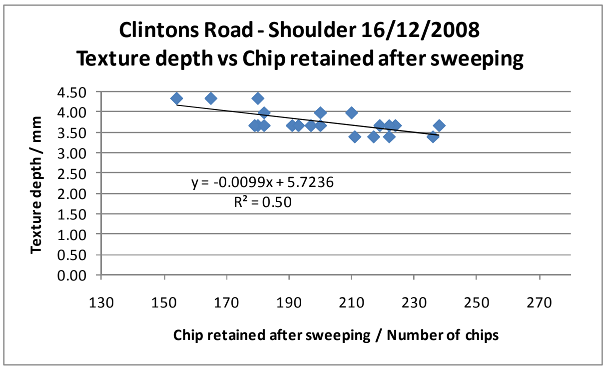
>0.10 ≤0.30 Weak relationship

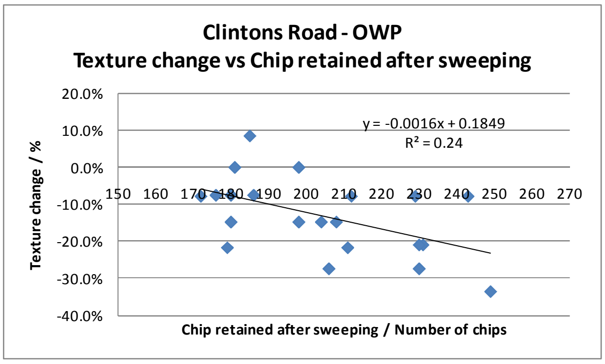
>0.30 ≤0.50 Average relationship

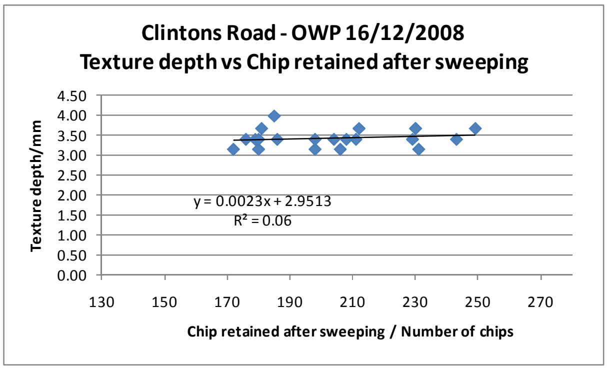
>0.50 ≤0.70 Good relationship

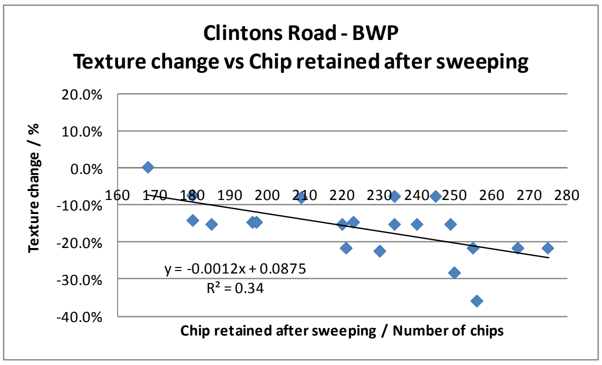
D1 Clintons Rd

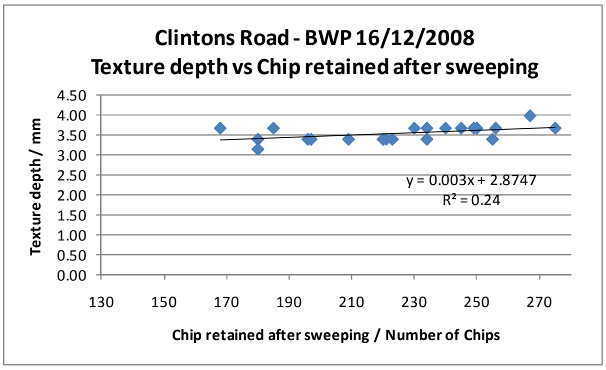


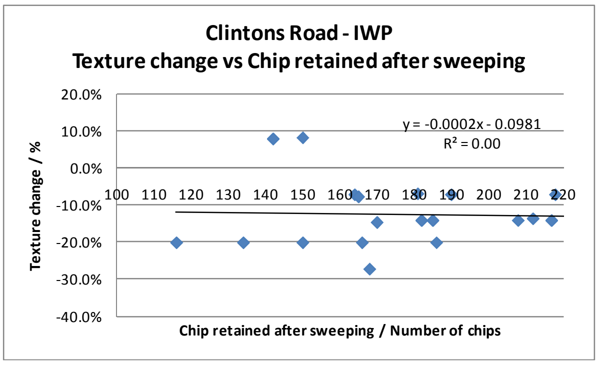


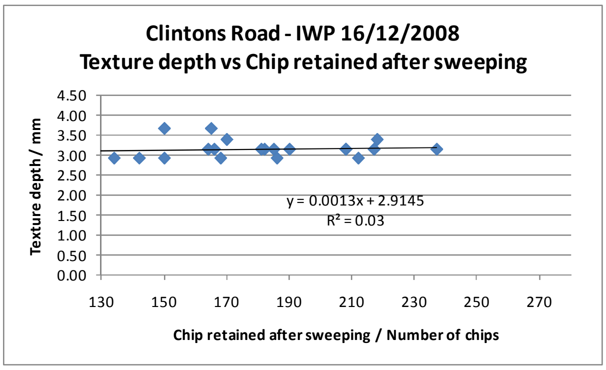




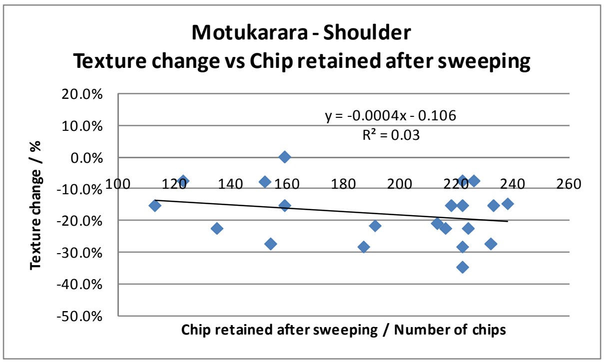


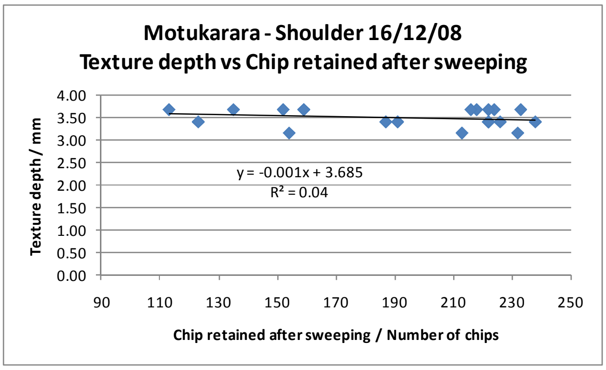


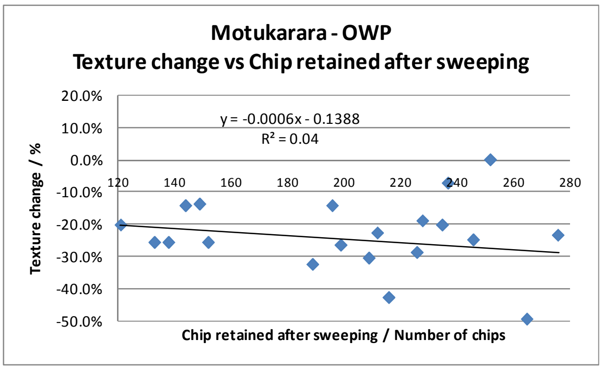


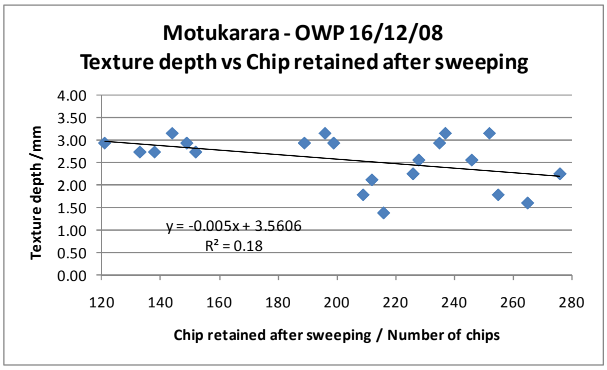


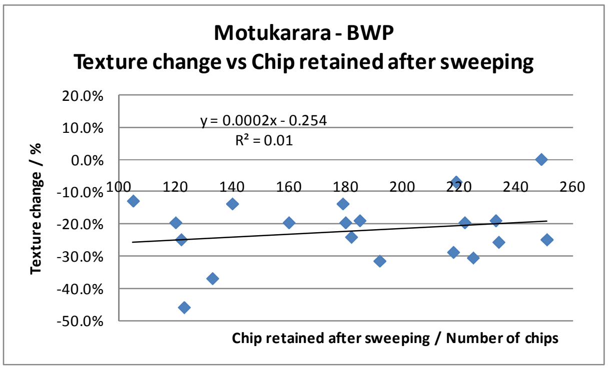
D2 Motukarara

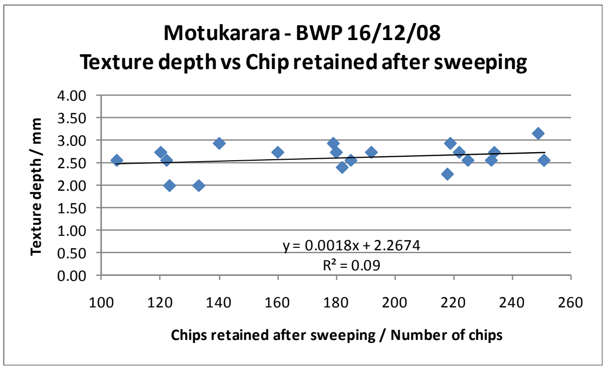


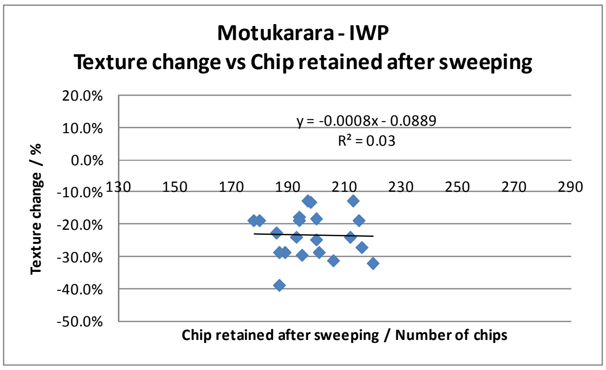


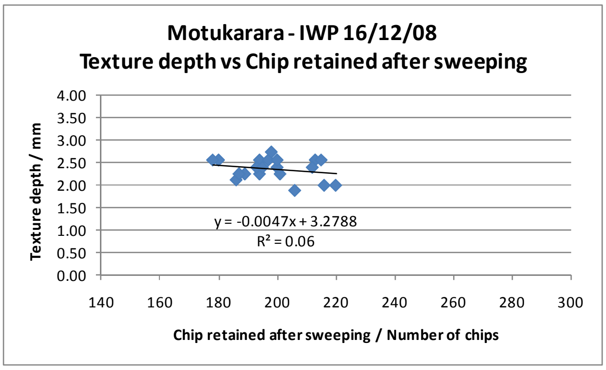




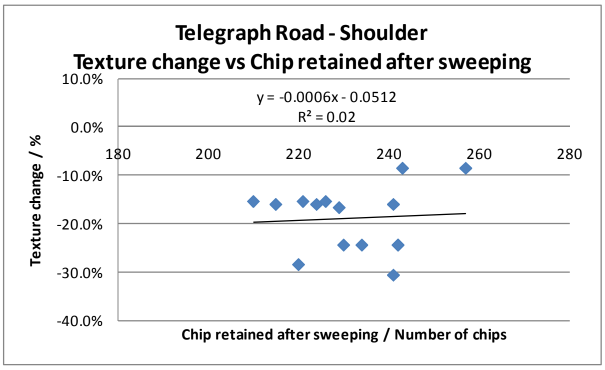


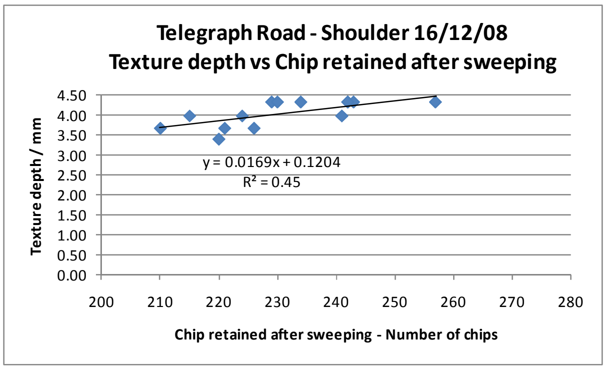


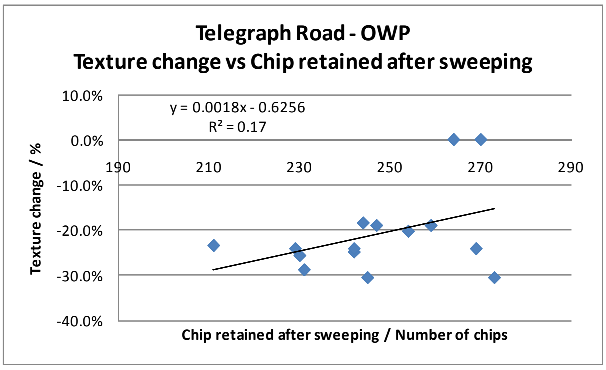


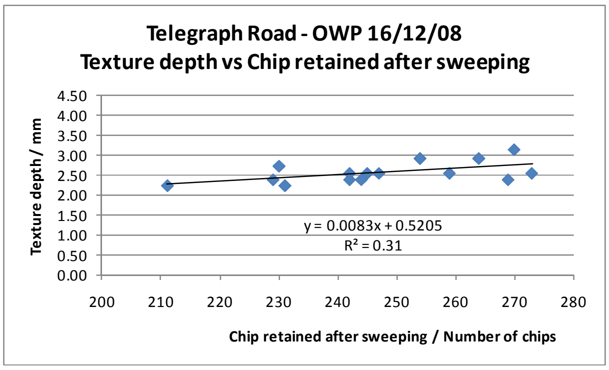


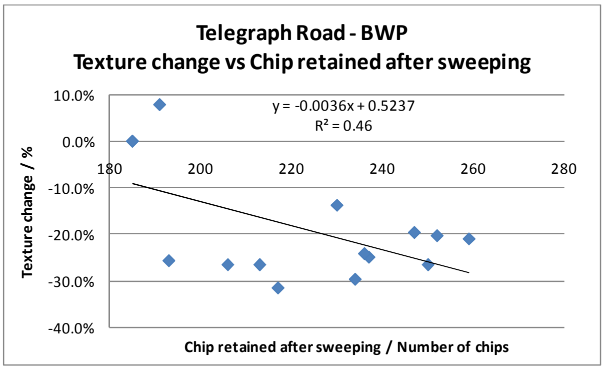
D3 Telegraph Rd

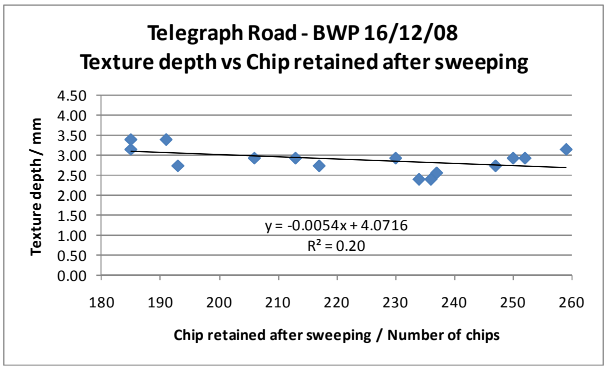


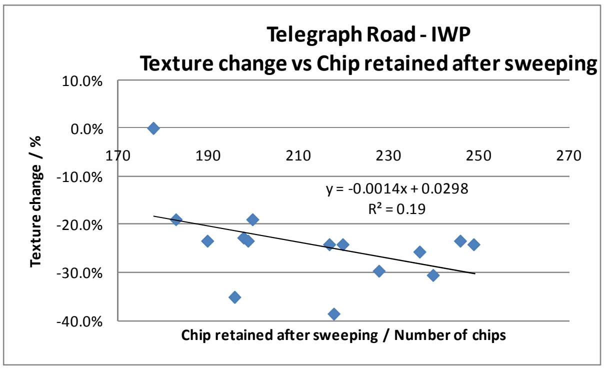


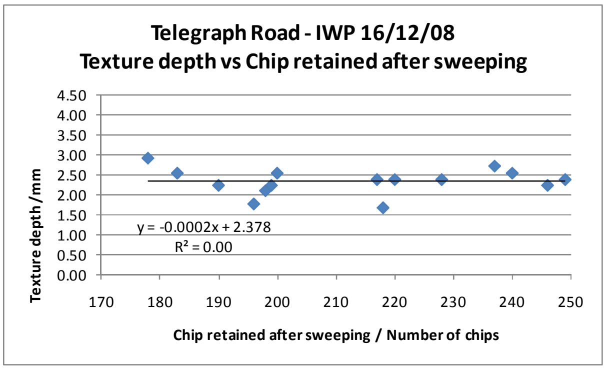




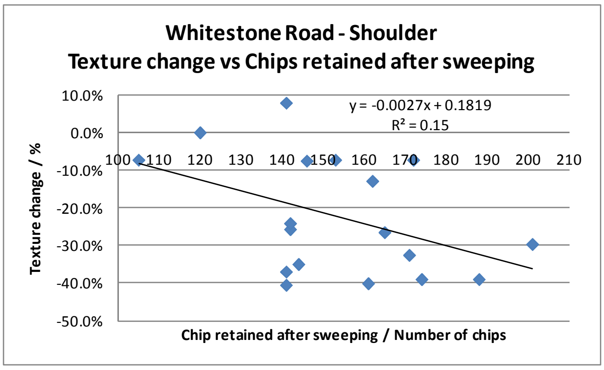


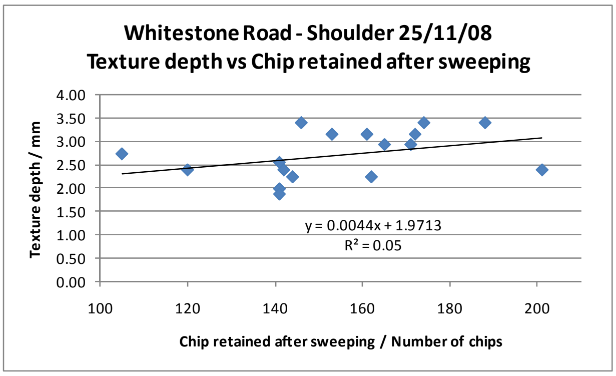


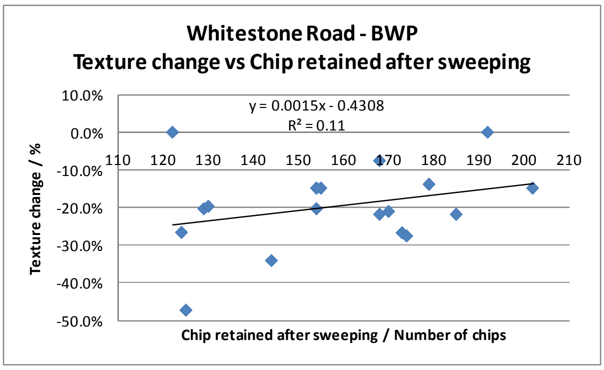


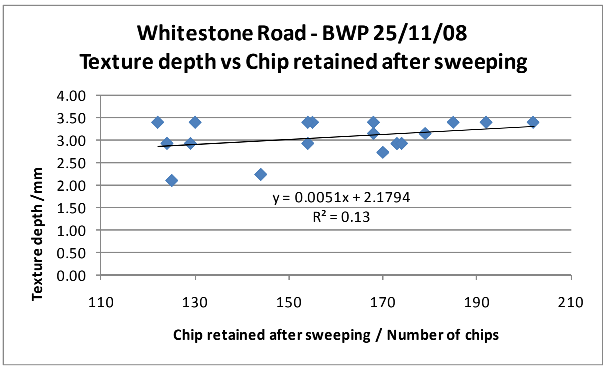


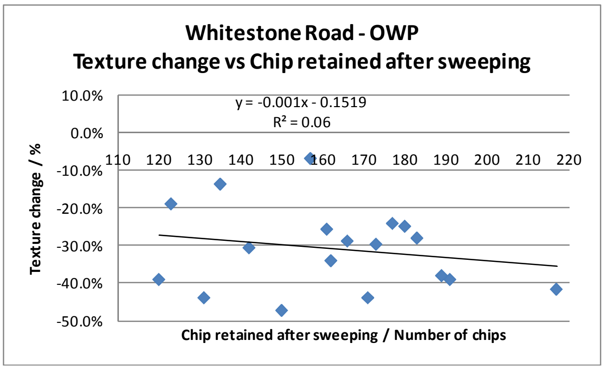
D4 Whitestone Rd

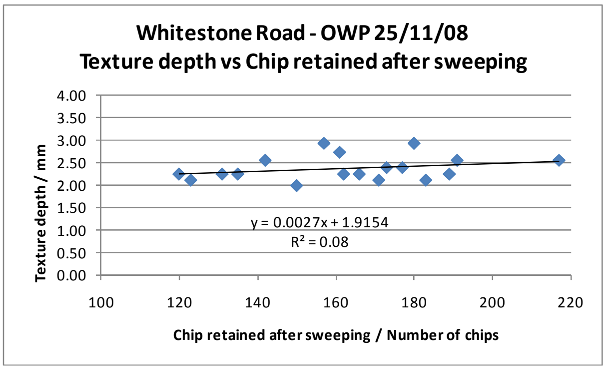


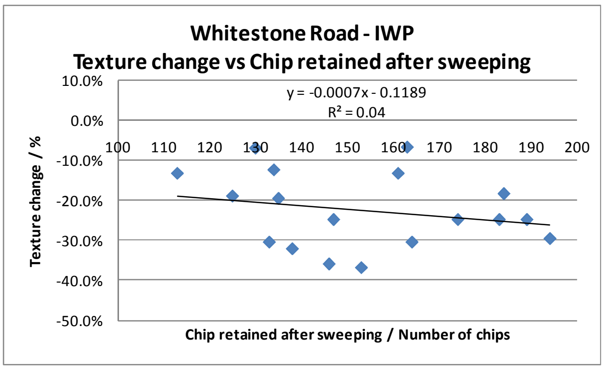


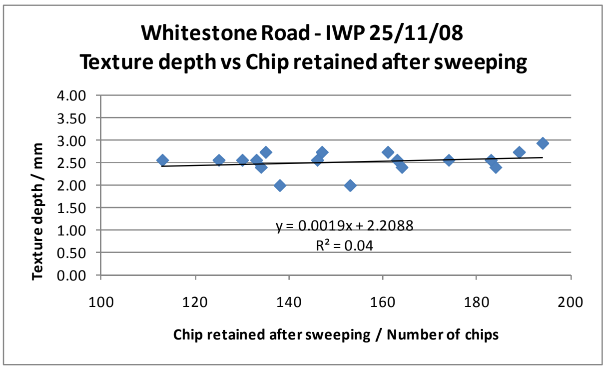




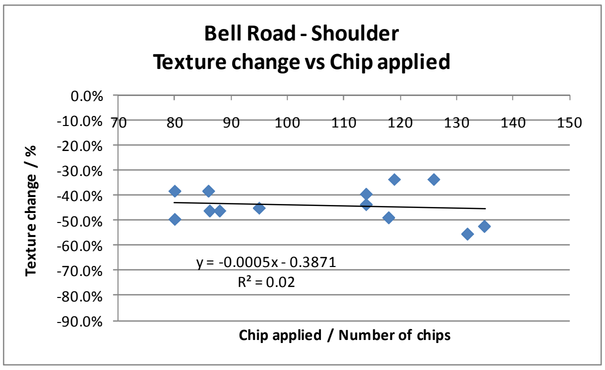


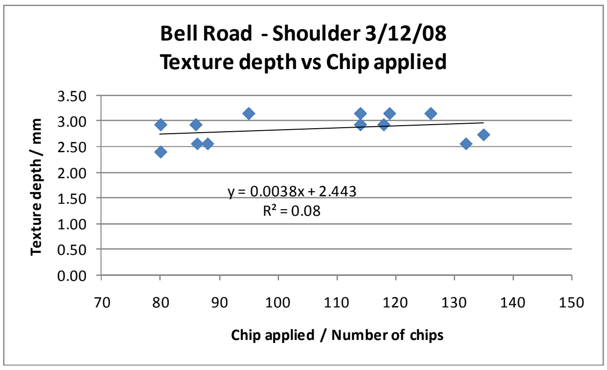


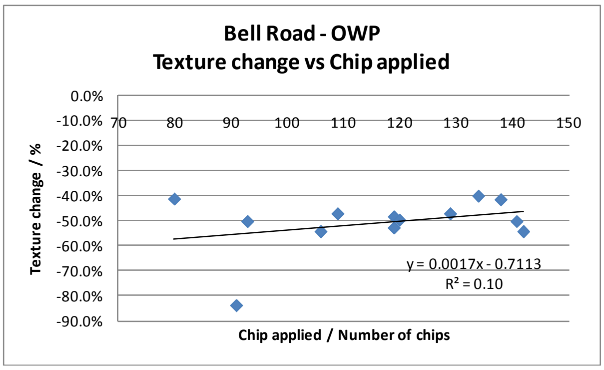


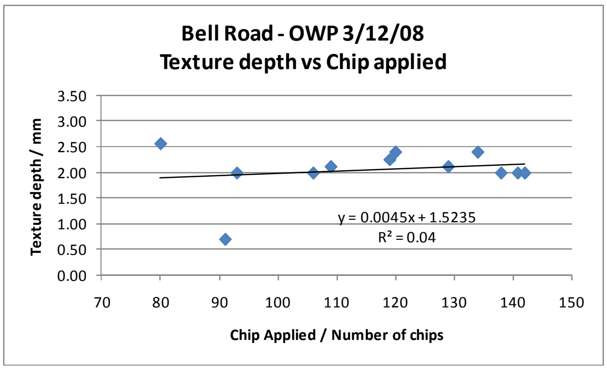


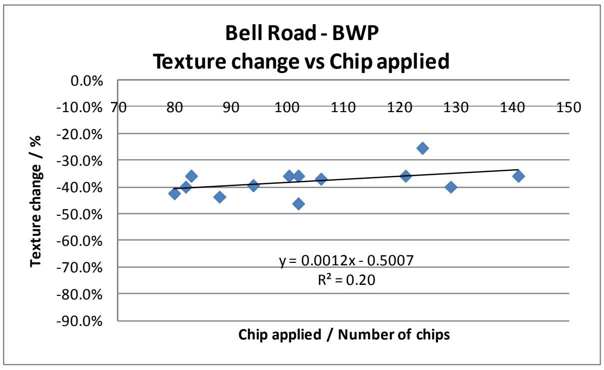
D5 Bell Rd

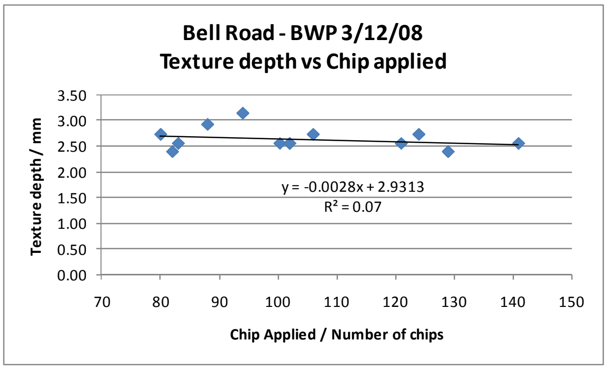

Bell Road - Shoulder
Texture change vs Chip applied
y = -0.0005x - 0.3871
R² = 0.02
Texture change / %
Chip applied / Number of chips

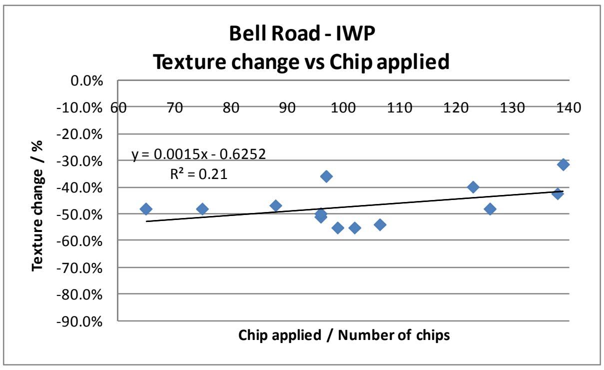

Bell Road - Shoulder 3/12/08
Texture depth vs Chip applied
y = 0.0038x + 2.443
R² = 0.08
Texture depth / mm
Chip applied / Number of chips

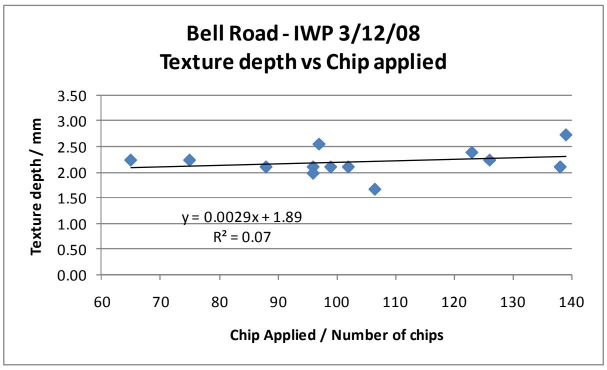

Bell Road - OWP
Texture change vs Chip applied
y = 0.0017x - 0.7113
R² = 0.10
Texture change / %
Chip applied / Number of chips


Bell Road - OWP 3/12/08
Texture depth vs Chip applied
y = 0.0045x + 1.5235
R² = 0.04
Texture depth / mm
Chip Applied / Number of chips

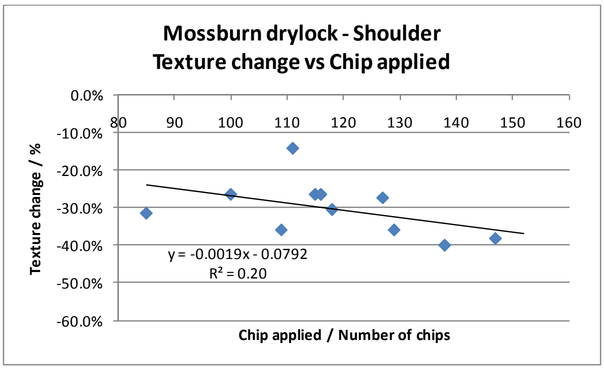

Bell Road - BWP
Texture change vs Chip applied
y = 0.0012x - 0.5007
R² = 0.20
Texture change / %
Chip applied / Number of chips

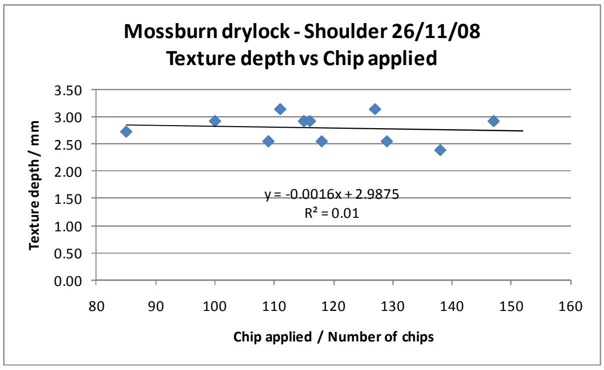

Bell Road - BWP 3/12/08
Texture depth vs Chip applied
y = -0.0028x + 2.9313
R² = 0.07
Texture depth / mm
Chip Applied / Number of chips

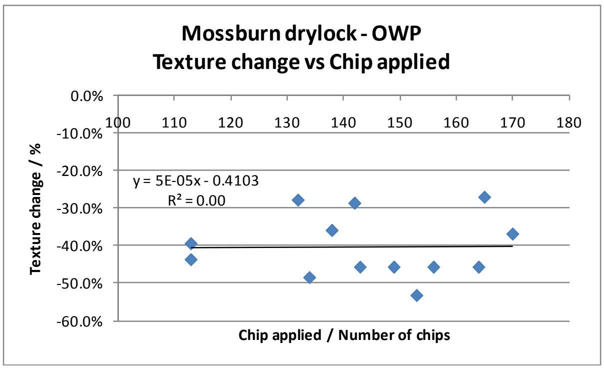

Bell Road - IWP
Texture change vs Chip applied
y = 0.0015x - 0.6252
R² = 0.21
Texture change / %
Chip applied / Number of chips

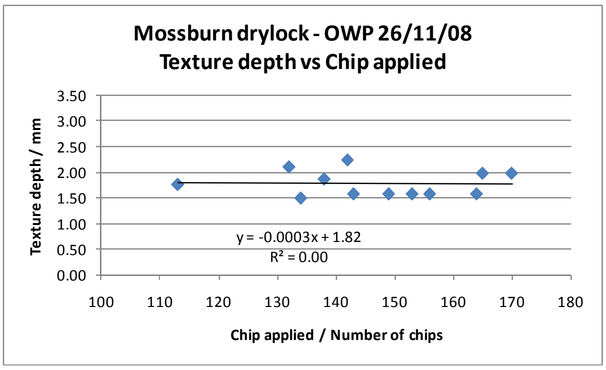

Bell Road - IWP 3/12/08
Texture depth vs Chip applied
y = 0.0029x + 1.89
R² = 0.07
Texture depth / mm
Chip Applied / Number of chips

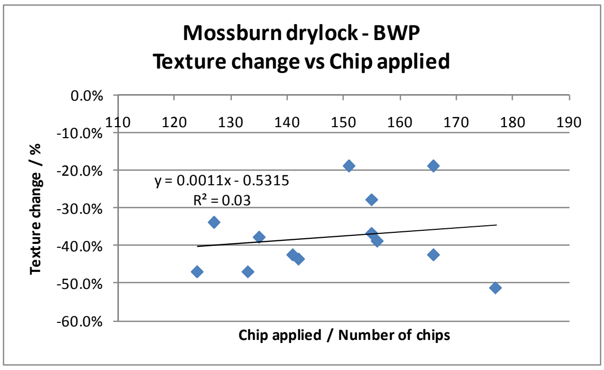
D6 Mossburn drylock

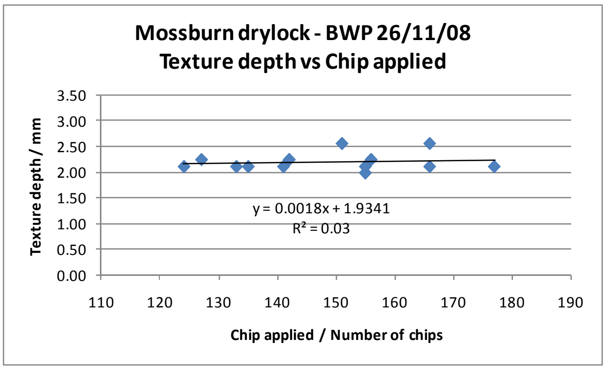


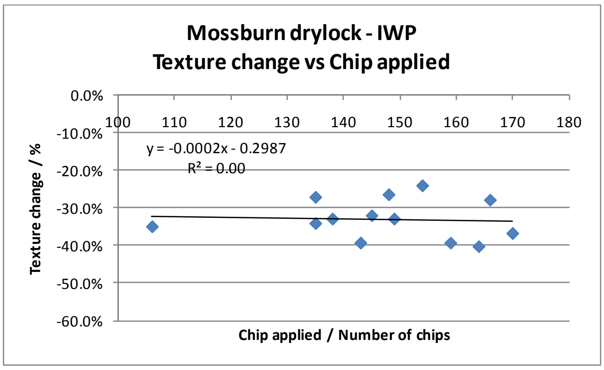


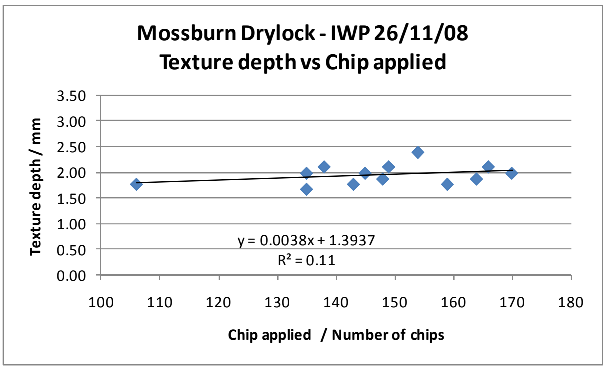




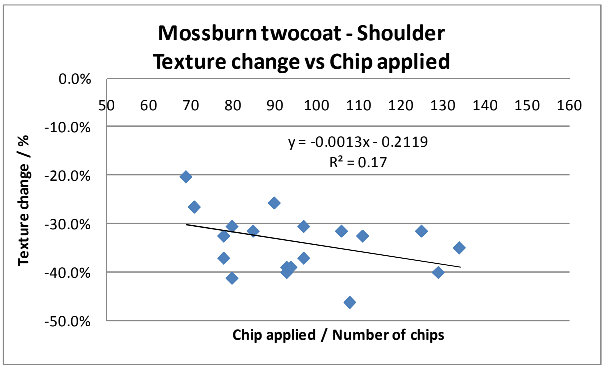


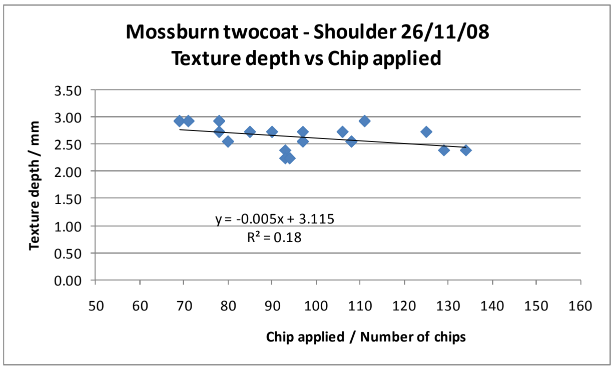


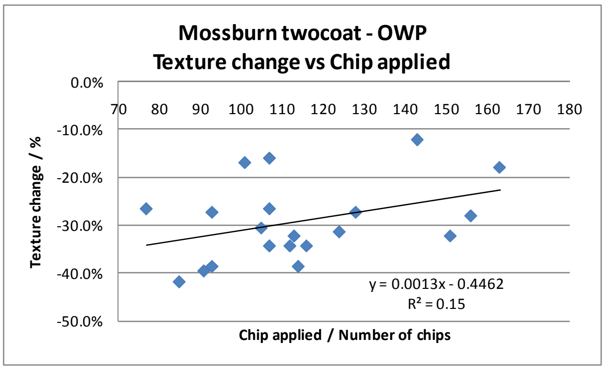


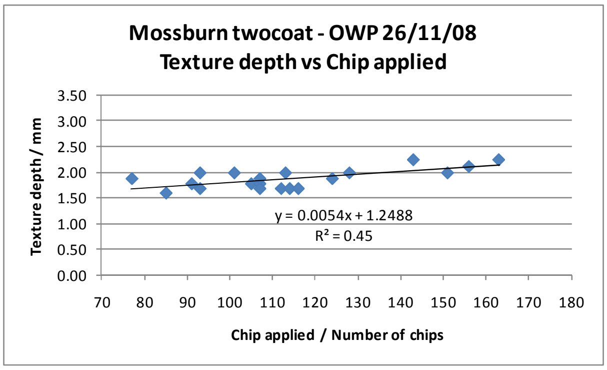


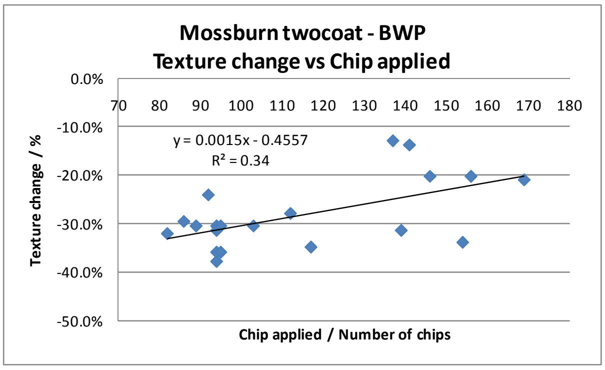
D7 Mossburn two-coat

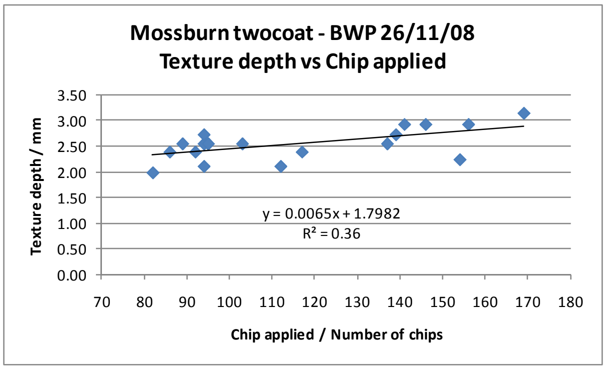


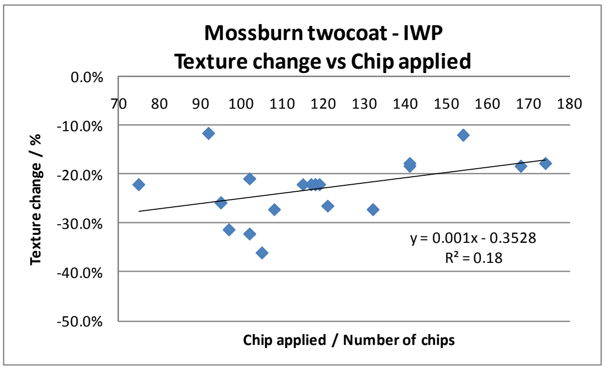


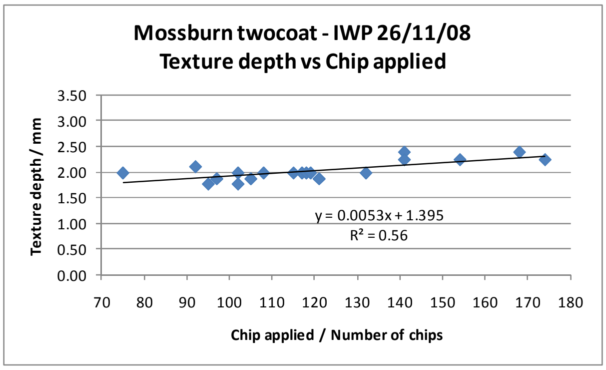












Appendix E: Chip application rate vs binder rise

E1 Summary

Table E1 Summary comparing binder rise at end of monitoring, with initial chip application rates

Site	Binder rise R^2	Binder rise category	Comment
Clintons Rd	0.18	Cat. 2 & Cat. 3	Weak, decr
Shoulder	0.00	Cat. 2	Nil
OWP	0.00	Cat. 2	Nil
BWP	0.00	Cat. 2	Nil
IWP	0.00	Cat. 3	Nil
Motukarara	0.10	Cat. 2 – Cat. 6	Weak, incr
Shoulder	0.00	Cat. 2	Nil
OWP	0.28	Cat. 2 – Cat. 6	Weak, incr
BWP	O.00	Cat. 2	Nil
IWP	0.09	Cat. 2 – Cat. 5	Nil
Telegraph Rd	0.04	Cat. 1 - Cat. 6	Nil
Shoulder	0.00	Cat. 1	Nil
OWP	0.25	Cat. 2 & Cat. 3	Weak, decr
BWP	0.07	Cat. 2 & Cat. 4	Nil
IWP	0.00	Cat. 2 – Cat. 6	Nil
Whitestone Rd	0.01	Cat. 2 – Cat. 6	Nil
Shoulder	0.10	Cat. 2 – Cat. 4	Weak, incr
OWP	0.18	Cat. 3 – Cat. 6	Weak, incr
BWP	0.09	Cat. 2 & Cat. 3	Nil
IWP	0.05	Cat. 3 – Cat. 5	Nil
Bell Rd	0.00	Cat. 3 – Cat. 7	Nil
Shoulder	0.14	Cat. 3 & Cat. 4	Weak, decr
OWP	0.50	Cat. 4 – Cat. 7	Good, decr
BWP	0.00	Cat. 3	Nil
IWP	0.02	Cat. 4 & Cat. 5	Nil
Mossburn drylock	0.10	Cat. 2 – Cat. 7	Nil
Shoulder	0.05	Cat. 2 – Cat. 4	Nil
OWP	0.16	Cat. 4 – Cat. 7	Weak, incr
BWP	0.00	Cat. 3	Nil
IWP	0.01	Cat. 4 & Cat. 5	Nil
Mossburn two-coat	0.00	Cat. 2 – Cat. 6	Nil
Shoulder	0.22	Cat. 2 & Cat. 3	Weak, decr
OWP	0.38	Cat. 4 – Cat. 6	Average, decr
BWP	0.26	Cat. 2 – Cat. 4	Weak, decr
IWP	0.08	Cat. 4 & Cat. 5	Nil

Coefficient of determination (R^2):

≤0.10 Nil relationship

>0.10 ≤0.30 Weak relationship

>0.30 ≤0.50 Average relationship

>0.50 ≤0.70 Good relationship

The study of the effect of the chip application rate on the binder rise in this research has shown that variation in chip application rates does not have an effect on the binder rise in chipseals in the first two years after construction. As expected, the binder rise in chipseal was affected more by the amount of trafficking and the state of the underlying surface.

E1.1 Clintons Rd

Table E2 Clintons Rd chip application rate vs binder rise 16/11/2008

Clintons Road chip retained after sweeping vs Binder Rise 16/12/2008								
	Shoulder		OWP		BWP		IWP	
Frame	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category
C1	182	2	204	2	230	2	208	3
C2	197	2	179	2	245	2	185	3
C3	191	2	211	2	221	2	170	3
H1	217	2	231	2	275	2	182	3
H2	211	2	230	2	255	2	166	3
H3	236	2	249	2	250	2	181	3
L1	180	2	172	2	234	2	164	3
L2	179	2	180	2	209	2	142	3
L3	200	2	198	2	220	2	168	3
N1	219	2	206	2	223	2	190	3
N2	224	2	212	2	249	2	186	3
N3	222	2	208	2	234	2	208	3
VH1	238	2	230	2	240	2	217	3
VH2	222	2	243	2	267	2	218	3
VH3	210	2	229	2	256	2	237	3
VL1	200	2	185	2	185	2	165	3
VL2	182	2	176	2	168	2	150	3
VL3	193	2	186	2	196	2	212	3
VVL1	154	2	198	2	197	2	116	3
VVL2	165	2	180	2	180	2	134	3
VVL3	180	2	181	2	180	2	150	3

Category is the proportion of binder rise up the chip:

Cat. 1 = ≤25%

Cat. 2 = >25%, ≤ 33.3%

Cat. 3 = >33.3%, ≤ 50%

Cat. 4 = >50%, ≤ 66.6%

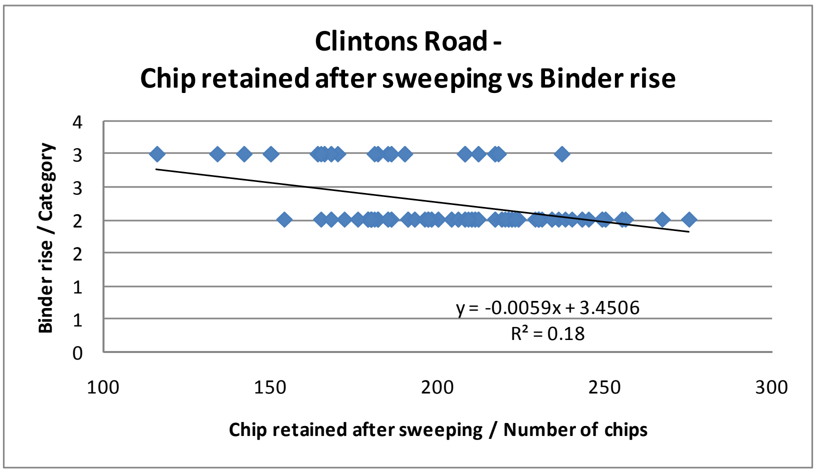
Cat. 5 = >66.6%, ≤75%

Cat. 6 = >75%, ≤90%

Cat. 7 = >90%

The binder rise measured at each frame at the final monitoring 22 months after seal construction was compared against the number of chips applied. The binder rise was all at category 2 for the shoulder, OWP and BWP, and all at category 3 for the IWP, regardless of the chip application rate. This suggested that on this site, binder rise was solely dependent on the trafficking, which was very light.

Figure E1 Graph comparing binder rise with chip application rate on the Clintons Rd site



E1.2 Motukarara

Table E3 Motukarara chip application rate vs binder rise 4/11/2008

Motukarara chip retained after sweeping vs Binder rise 4/11/2008								
	Shoulder		OWP		BWP		IWP	
Frame	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category
C1	238	2	235	2	234	2	213	2
C2	224	2	237	2	251	2	212	2
C3	222	2	252	2	251	2	215	2
H1	222	2	276	3	233	2	186	3
H2	222	2	226	3	219	2	189	3
H3	226	2	228	3	192	2	194	3
L1	154	2	189	2	182	2	180	2
L2	187	2	196	2	218	2	178	2
L3	191	2	199	2	185	2	194	2
N1	213	2	216	5	180	2	197	3
N2	218	2	209	5	179	2	200	3
N3	233	2	212	5	160	2	187	3
VH1	232	2	246	5	222	2	201	3
VH2	216	2	265	6	225	2	216	5
VH3	222	2	255	5	249	2	220	3
VL1	152	2	138	2	105	2	206	5
VL2	159	2	152	2	140	2	200	2
VL3	135	2	133	2	133	2	198	2
VVL1	123	2	149	2	120	2	187	2
VVL2	159	2	121	2	122	2	193	2
VVL3	113	2	144	2	123	2	195	2

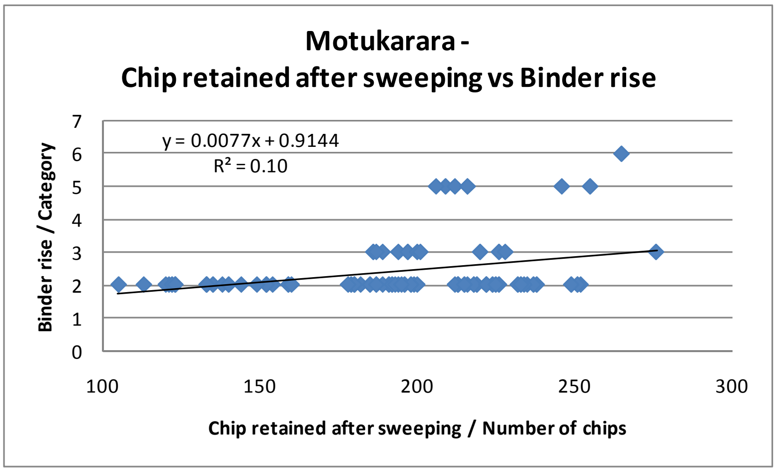
The binder rise measured at each frame at the final monitoring 20 months after seal construction was compared against the number of chips applied.

The binder rise was all category 2 for the shoulder and BWP (which are the lower-trafficked areas), with no discernable difference caused by the chip application rate.

There was some variation in the wheelpaths, so this data was graphed.

The binder rise in the OWP frames also showed an increase with increased chip application rate, with a weak relationship ($r^2 = 0.28$) between the data.

Figure E2 Graph comparing binder rise with chip application for the Motukarara site



E1.3 Telegraph Rd

Table E4 Telegraph Rd chip application rate vs binder rise 18/12/2008

Telegraph Road chip retained after sweeping vs Binder rise 18/12/2008								
	Shoulder		OWP		BWP		IWP	
Frame	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category
C1	221	1	247	2	237	4	196	6
C2	224	1	242	2	234	4	198	5
C3	215	1	259	2	236	4	218	6
H1	241	1	244	3	252	2	237	3
H2	257	1	242	3	259	2	249	3
H3	243	1	229	3	250	2	240	3
L1	229	1	230	2	193	2	190	4
L2	234	1	245	2	206	2	217	4
L3	242	1	270	2	213	2	199	4
N1	241	1	273	2	247	2	228	3
N2	242	1	269	2	230	2	246	3
N3	230	1	254	2	217	2	220	3
VL1	226	1	211	3	185	2	183	2
VL2	220	1	264	3	185	2	178	2
VL3	210	1	231	3	191	2	200	2

The binder rise measured at each frame at the final monitoring 22 months after seal construction was compared against the number of chips applied.

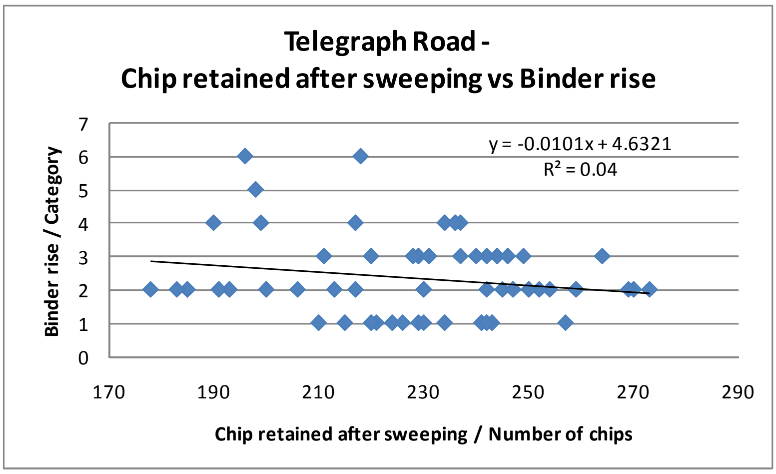
The binder rise was all category 1 in the shoulder frames, which were outside the edgeline on a small shoulder, so there was probably very little trafficking. There was no discernible difference caused by the various chip application rates.

The binder rise in the BWP frames was all category 2 apart from the frames in the control section, which were category 4. It is possible that the extra rise in the control section was caused by having less texture on the previous surface before sealing.

The binder rise in the OWP showed some variation between category 2 and category 3, with a weak relationship ($r^2 = 0.25$) showing binder rise increasing with a decreasing chip application rate.

The binder rise in the IWP ranged from category 2 to category 6, with no relationship ($r^2 = 0.00$) between binder rise and the chip application rate.

Figure E3 Graph comparing binder rise with chip application on the Telegraph Rd site



E1.4 Whitestone Rd

Table E5 Whitestone Rd chip application rate vs binder rise 25/11/2008

Whitestone Road chip retained after sweeping vs Binder rise 25/11/2008								
	Shoulder		OWP		BWP		IWP	
Frame	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category
C1	172	4	166	4	192	2	183	5
C2	201	3	173	4	185	2	184	4
C3	171	3	183	4	202	2	174	4
H1	142	3	150	5	179	2	147	4
H2	144	2	171	5	168	2	146	3
H3	162	3	191	6	168	2	164	3
L1	105	3	123	3	129	3	133	4
L2	120	3	120	3	122	2	113	4
L3	141	3	135	3	130	2	130	5
N1	165	2	142	3	124	2	153	4
N2	146	2	161	3	155	2	135	4
N3	153	2	131	3	173	2	161	3
VH1	161	4	217	3	174	2	163	3
VH2	188	4	189	5	154	2	189	3
VH3	174	4	180	4	170	2	194	3
VL1	141	3	157	3	125	2	125	3
VL2	141	3	177	3	144	2	138	4
VL3	142	3	162	3	154	2	134	4

The binder rise measured at each frame at the final monitoring 22 months after seal construction was compared against the number of chips applied. There were signs that the binder flowed towards the outside of the lane on sites on the bend – ie the C, H, and VH sections.

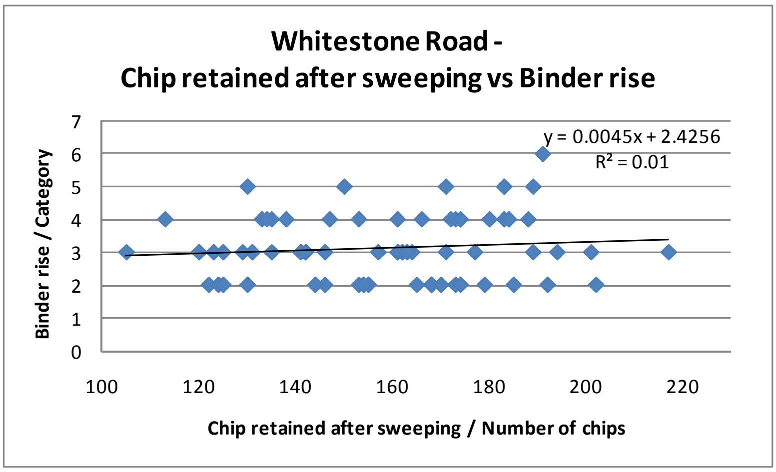
The binder rise in the shoulder frames varied between category 2 and category 4. On this site the C, H, and VH shoulder frames were on the inside of a large radius curve, so there would have been more trafficking, especially in the H and VH frames, which were on the start of the bend. There was a weak relationship ($r^2 = 0.10$) between increasing binder rise and an increasing chip application rate.

The binder rise in the OWP showed some variation between category 3 and category 6, with a weak relationship ($r^2 = 0.18$) showing binder rise increasing with an increasing chip application rate.

The binder rise in the BWP showed no relationship between binder rise and chip application rate – all frames except L1 (which was category 3) were category 2 for binder rise.

The binder rise in the IWP showed some variation between category 3 and category 5, with no relationship ($r^2 = 0.05$) between binder rise and chip application rate.

Figure E4 Graph comparing binder rise with chip application on the Whitestone Rd site



E1.5 Bell Rd

Table E6 Telegraph Rd chip application rate vs binder rise 13/12/2008

Bell Road chip application vs Binder rise 3/12/2008								
	Shoulder		OWP		BWP		IWP	
Frame	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category
C1	86	3	141	5	100	3	106	5
HH1	126	3	134	4	121	3	138	5
HH2	119	3	138	4	141	3	123	5
HL1	135	3	142	5	124	3	139	4
HL2	132	3	129	4	129	3	126	4
NH1	114	3	119	4	106	3	96	5
NH2	95	3	120	4	102	3	97	4
NL1	118	3	119	4	94	3	102	5
NL2	114	3	109	5	102	3	99	5
LH1	80	3	106	5	82	3	88	5
LH2	88	3	93	5	83	3	96	5
LL1	86	3	80	7	88	3	75	4
LL2	80	4	91	7	80	3	65	4

The binder rise measured at each frame at the final monitoring 24 months after seal construction was compared against the number of chips applied.

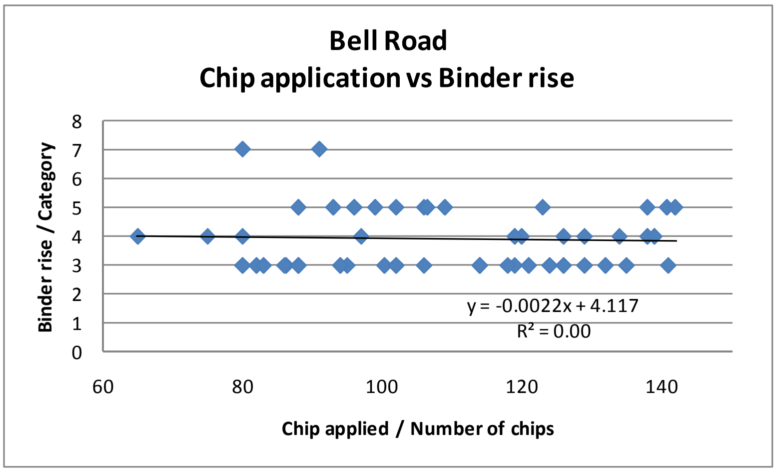
Apart from LL2, which was category 4, the binder rise in the shoulder frames was all category 3 – this showed there was no relationship between binder rise and chip application rate.

The binder rise in the OWP showed some variation between category 4 and category 7, with an average relationship ($r^2 = 0.50$) showing binder rise decreasing with an increased chip application rate.

The binder rise in the BWP frames was all category 3 – this showed there was no relationship between binder rise and chip application rate.

The binder rise in the IWP showed some variation between category 4 and category 5, with no relationship between binder rise and chip application rate.

Figure E5 Graph comparing binder rise with chip application for the Bell Rd site



E1.6 Mossburn drylock

Table E7 Mossburn drylock chip application rate vs binder rise 26/11/2008

Mossburn drylock chip application vs Binder rise 26/11/2008								
	Shoulder		OWP		BWP		IWP	
Frame	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category
C1	127	4	132	4	142	3	135	5
C2	152	4	153	6	133	3	164	5
H1	127	3	170	5	166	3	170	4
H2	147	2	165	5	166	3	166	4
H3	116	3	142	5	177	3	154	4
L1	118	3	113	5	156	3	148	4
L2	100	3	138	4	127	3	143	4
L3	85	3	113	5	135	3	106	4
N1	109	2	143	5	124	3	138	4
N2	115	3	164	7	141	3	149	5
N3	111	2	156	5	151	3	135	4
NH1	138	3	134	5	155	3	145	4
NH2	129	3	149	5	155	3	159	4

The binder rise measured at each frame at the final monitoring 24 months after seal construction was compared against the number of chips applied.

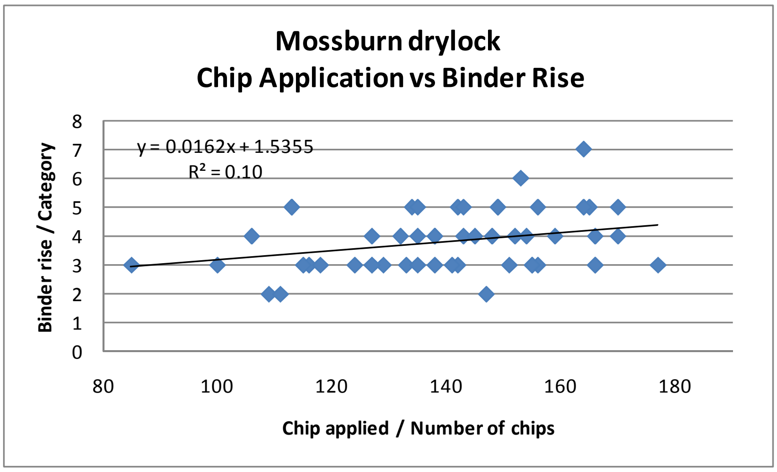
The binder rise in the shoulder frames showed some variation between category 2 and category 4, but there was no relationship between binder rise and chip application rate.

The binder rise in the OWP showed some variation between category 4 and category 7, with a weak relationship ($r^2 = 0.16$) showing binder rise increasing with increasing chip application rate.

The binder rise in the BWP frames was all category 3 – this showed there was no relationship between binder rise and chip application rate.

The binder rise in the IWP showed some variation between category 4 and category 5, with no relationship between binder rise and chip application rate.

Figure E6 Graph comparing binder rise and chip application on Mossburn drylock site



E1.7 Mossburn two-coat

Table E8 Mossburn two-coat chip application rate vs binder rise 26/11/2008

Mossburn Twocoat Chip Application vs Binder Rise 26/11/2008								
	Shoulder		OWP		BWP		IWP	
Frame	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category	Number of chips	Binder rise category
C1	93	3	93	5	95	2	97	5
C2	94	3	91	5	89	2	102	5
HH1	106	2	143	5	137	2	141	5
HH2	97	3	128	4	139	2	141	4
HH3	111	2	101	5	141	2	132	4
HL1	134	2	151	4	156	2	154	4
HL2	125	3	163	4	146	2	168	4
HL3	129	2	156	4	169	2	174	4
LH1	108	2	112	4	154	3	118	4
LH2	80	2	107	5	86	3	117	4
LH3	78	2	107	4	92	3	92	4
LL1	71	3	93	6	82	3	75	4
LL2	71	3	85	6	112	4	102	5
LL3	85	3	107	6	94	3	95	4
NH1	97	3	124	4	95	3	105	5
NH2	78	3	77	5	94	3	108	5
NH3	80	3	113	5	103	3	121	4
NL1	90	3	116	5	117	3	119	4
NL2	93	3	105	5	94	3	118	4
NL3	69	3	114	4	94	3	115	4

The binder rise measured at each frame at the final monitoring 24 months after seal construction was compared against the number of chips applied.

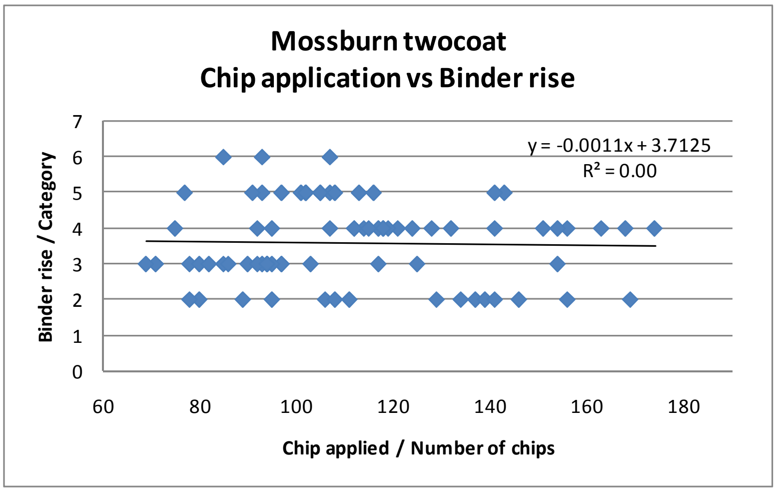
The binder rise in the shoulder frames showed some variation between category 2 and category 3, with a weak relationship ($r^2 = 0.22$) showing binder rise decreasing with increasing chip application rate.

The binder rise in the OWP showed some variation between category 4 and category 6, with an average relationship ($r^2 = 0.38$) showing binder rise decreasing with increasing chip application rate.

The binder rise in the BWP frames showed some variation between category 2 and category 4, with a weak relationship ($r^2 = 0.26$) showing binder rise decreasing with increasing chip application rate.

The binder rise in the IWP showed some variation between category 4 and category 5, with no relationship ($r^2 = 0.08$) between binder rise and chip application rate.

Figure E7 Graph comparing binder rise with chip application on Mossburn two-coat site



Appendix F: Chip application rate vs chip breakdown

Table F1 Chip application rate vs chip breakdown

Site	% broken chip (on site) R^2	Comment	% broken chip (off photos) R^2	Comment
Clintons Rd	0.04	Nil	0.05	Nil
Shoulder	0.33	Average, decr	0.27	Weak, decr
OWP	0.11	Weak, decr	0.02	Nil
BWP	0.01	Nil	0.07	Nil
IWP	0.00	Nil	0.16	Weak, incr
Motukarara	0.04	Nil	0.03	Nil
Shoulder	0.14	Weak, decr	0.09	Nil
OWP	0.08	Nil	0.03	Nil
BWP	0.16	Weak, incr	0.17	Weak, incr
IWP	0.08	Nil	0.02	Nil
Telegraph Rd	0.00	Nil	0.00	Nil
Shoulder	0.14	Weak, decr	0.00	Nil
OWP	0.03	Nil	0.00	Nil
BWP	0.00	Nil	0.05	Nil
IWP	0.00	Nil	0.12	Weak, incr
Whitestone Rd	0.03	Nil	0.03	Nil
Shoulder	0.49	Average, incr	0.44	Average, incr
OWP	0.01	Nil	0.05	Nil
BWP	0.00	Nil	0.07	Nil
IWP	0.00	Nil	0.02	Nil
Bell Rd Shoulder OWP BWP IWP	N/A	N/A	N/A	N/A
Mossburn drylock	0.13	Weak, decr	N/A	N/A
Shoulder	0.06	Nil		
OWP	0.20	Weak, decr		
BWP	0.03	Nil		
IWP	0.21	Weak, incr		
Mossburn two-coat Shoulder OWP BWP IWP	N/A	N/A	N/A	N/A

Coefficient of determination (R^2):

≤ 0.10 Nil relationship

$>0.10 \leq 0.30$ Weak relationship

$>0.30 \leq 0.50$ Average relationship

$>0.50 \leq 0.70$ Good relationship